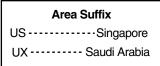
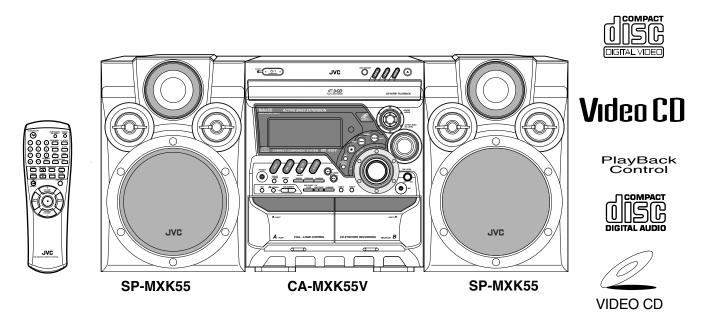
# JVC SERVICE MANUAL COMPACT COMPONENT SYSTEM

# **MX-K55V**





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### -Safety Precautions

- 1. This design of this product contains special hardware and many circuits and components specially for safety purposes. For continued protection, no changes should be made to the original design unless authorized in writing by the manufacturer. Replacement parts must be identical to those used in the original circuits. Services should be performed by qualified personnel only.
- 2. Alterations of the design or circuitry of the product should not be made. Any design alterations of the product should not be made. Any design alterations or additions will void the manufacturer's warranty and will further relieve the manufacture of responsibility for personal injury or property damage resulting therefrom.
- 3. Many electrical and mechanical parts in the products have special safety-related characteristics. These characteristics are often not evident from visual inspection nor can the protection afforded by them necessarily be obtained by using replacement components rated for higher voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in the Parts List of Service Manual. Electrical components having such features are identified by shading on the schematics and by (A) on the Parts List in the Service Manual. The use of a substitute replacement which does not have the same safety characteristics as the recommended replacement parts shown in the Parts List of Service Manual may create shock, fire, or other hazards.
- 4. The leads in the products are routed and dressed with ties, clamps, tubings, barriers and the like to be separated from live parts, high temperature parts, moving parts and/or sharp edges for the prevention of electric shock and fire hazard. When service is required, the original lead routing and dress should be observed, and it should be confirmed that they have been returned to normal, after re-assembling.
- 5. Leakage current check (Electrical shock hazard testing)

After re-assembling the product, always perform an isolation check on the exposed metal parts of the product (antenna terminals, knobs, metal cabinet, screw heads, headphone jack, control shafts, etc.) to be sure the product is safe to operate without danger of electrical shock.

Do not use a line isolation transformer during this check.

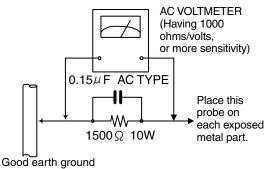
Plug the AC line cord directly into the AC outlet. Using a "Leakage Current Tester", measure the leakage current from each exposed metal parts of the cabinet, particularly any exposed metal part having a return path to the chassis, to a known good earth ground. Any leakage current must not exceed 0.5mA AC (r.m.s.).

#### Alternate check method

Plug the AC line cord directly into the AC outlet. Use an AC voltmeter having, 1,000 ohms per volt or more sensitivity in the following manner. Connect a 1,500  $\Omega$  10W resistor paralleled by a 0.15 $\mu$ F AC-type capacitor

between an exposed metal part and a known good earth ground. Measure the AC voltage across the resistor with the AC voltmeter.

Move the resistor connection to each exposed metal part, particularly any exposed metal part having a return path to the chassis, and measure the AC voltage across the resistor. Now, reverse the plug in the AC outlet and repeat each measurement. Voltage measured any must not exceed 0.75 V AC (r.m.s.). This corresponds to 0.5 mA AC (r.m.s.).



#### Warning

- 1. This equipment has been designed and manufactured to meet international safety standards.
- 2. It is the legal responsibility of the repairer to ensure that these safety standards are maintained.
- 3. Repairs must be made in accordance with the relevant safety standards.
- 4. It is essential that safety critical components are replaced by approved parts.
- 5. If mains voltage selector is provided, check setting for local voltage.

Burrs formed during molding may be left over on some parts of the chassis. Therefore, pay attention to such burrs in the case of preforming repair of this system.

In regard with component parts appearing on the silk-screen printed side (parts side) of the PWB diagrams, the parts that are printed over with black such as the resistor (--), diode (+-) and ICP (-) or identified by the " $\underline{\wedge}$ " mark nearby are critical for safety.

When replacing them, be sure to use the parts of the same type and rating as specified by the manufacturer. (Except the J&C version)

# Preventing static electricity

#### 1. Grounding to prevent damage by static electricity

Electrostatic discharge (ESD), which occurs when static electricity stored in the body, fabric, etc. is discharged, can destroy the laser diode in the traverse unit (optical pickup). Take care to prevent this when performing repairs.

#### 2. About the earth processing for the destruction prevention by static electricity

In the equipment which uses optical pick-up (laser diode), optical pick-up is destroyed by the static electricity of the work environment.

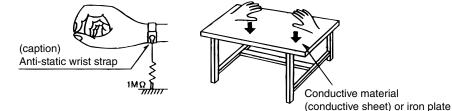
Be careful to use proper grounding in the area where repairs are being performed.

#### 2-1 Ground the workbench

Ground the workbench by laying conductive material (such as a conductive sheet) or an iron plate over it before placing the traverse unit (optical pickup) on it.

#### 2-2 Ground yourself

Use an anti-static wrist strap to release any static electricity built up in your body.



#### 3. Handling the optical pickup

- 1. In order to maintain quality during transport and before installation, both sides of the laser diode on the replacement optical pickup are shorted. After replacement, return the shorted parts to their original condition. (Refer to the text.)
- 2. Do not use a tester to check the condition of the laser diode in the optical pickup. The tester's internal power source can easily destroy the laser diode.

#### 4. Handling the traverse unit (optical pickup)

- 1. Do not subject the traverse unit (optical pickup) to strong shocks, as it is a sensitive, complex unit.
- 2. Cut off the shorted part of the flexible cable using nippers, etc. after replacing the optical pickup. For specific details, refer to the replacement procedure in the text. Remove the anti-static pin when replacing the traverse unit. Be careful not to take too long a time when attaching it to the connector.
- 3. Handle the flexible cable carefully as it may break when subjected to strong force.
- 4. It is not possible to adjust the semi-fixed resistor that adjusts the laser power. Do not turn it

#### Attention when CD mechanism assembly is decomposed

- \*Please refer to "Disassembly method" in the text for pick-up and how to detach the CD mechanism assembly.
- Card wire 1. Remove the CD changer unit. Pickup unit 2. Remove the CD holder mechanism. connector CD holder 3. Solder is put up before the card wire is removed from the pickup unit mechanism connector on the CD mechanism assembly. Fig.1 (When the card wire is removed without putting up solder, the CD pick-up Card wire assembly might destroy.) 4. Please remove solder after connecting the card wire with the pickup unit connector when you install picking up in the substrate. Soldering Pickup unit

CD changer unit

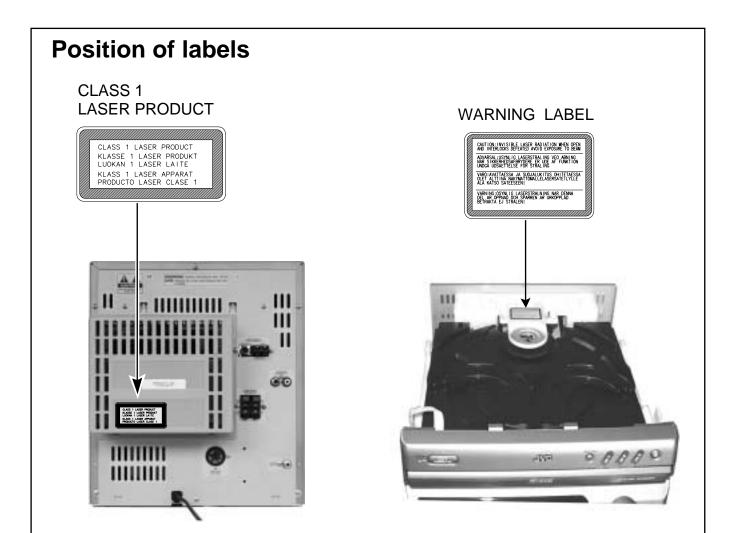
connector Fig.2

# Important for laser products

#### **1.CLASS 1 LASER PRODUCT**

- **2.DANGER :** Invisible laser radiation when open and inter lock failed or defeated. Avoid direct exposure to beam.
- **3.CAUTION :** There are no serviceable parts inside the Laser Unit. Do not disassemble the Laser Unit. Replace the complete Laser Unit if it malfunctions.
- **4.CAUTION :** The compact disc player uses invisible laserradiation and is equipped with safety switches whichprevent emission of radiation when the drawer is open and the safety interlocks have failed or are de feated. It is dangerous to defeat the safety switches.
- **5.CAUTION :** If safety switches malfunction, the laser is able to function.
- **6.CAUTION :** Use of controls, adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

A CAUTION Please use enough caution not to see the beam directly or touch it in case of an adjustment or operation check.



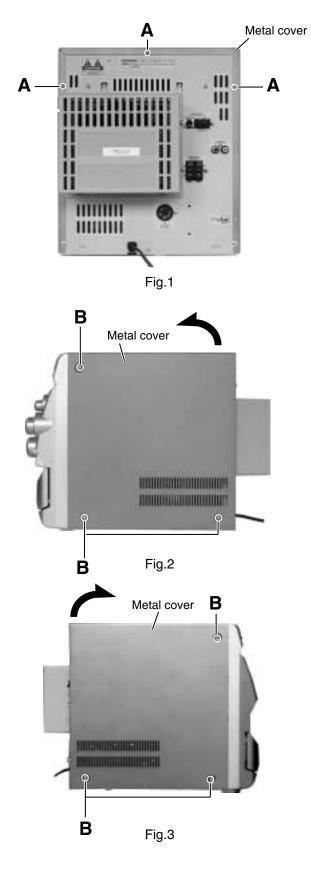
# **Disassembly method**

#### <Main body>

#### Removing the metal cover

#### (See Fig.1 to 3)

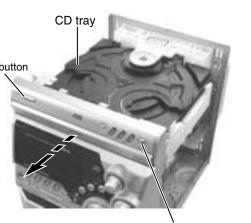
- 1. Remove the three screws **A** attaching the metal cover on the back of the body.
- 2. Remove the six screws **B** attaching the metal cover on both sides of the body.
- 3. Remove the metal cover from the body by lifting the rear part of the cover.
  - ATTENTION: Do not break the front panel tab fitted to the metal cover.



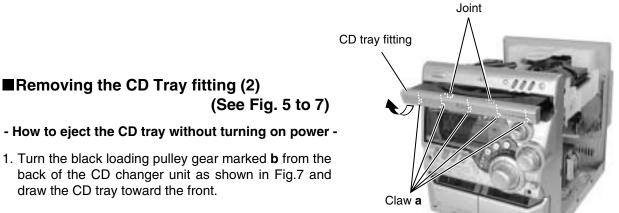
#### MX-K55V

#### Removing the CD Tray fitting (1) (See Fig. 4 to 6)

- Prior to performing the following procedure, remove POWER button the metal cover.
- 1. Press the POWER button. Press the OPEN/CLOSE button to eject the CD tray.
- 2. After drawing the lower part of the tray fitting toward the front, remove the five claws a. Then, while moving the tray fitting upward, remove it.
- 3. Press the OPEN/CLOSE button to insert the tray.



**OPEN/CLOSE** button Fig.4



2. After drawing the lower part of the tray fitting toward the front, remove the five claws a. Then, while moving the tray fitting upward, remove it.

3. Push and insert the CD tray manually.

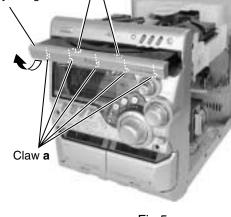
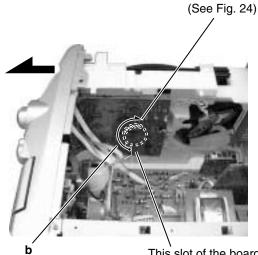


Fig.5



(Loading pulley gear)

This slot of the board.

Fig.7

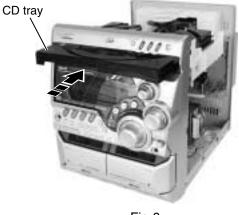
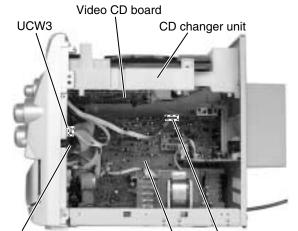


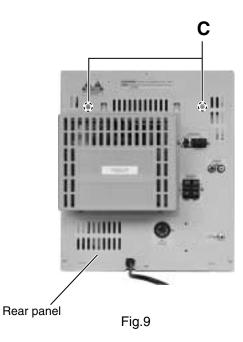
Fig.6

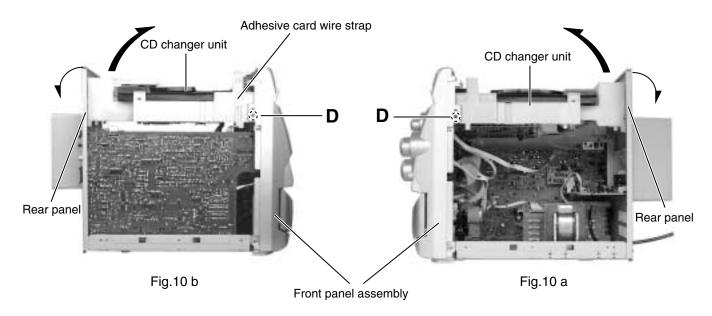
#### Removing the CD changer unit (See Fig.8 to 10)

- Prior to performing the following procedure, remove the metal cover.
- 1. Disconnect the card wire which is attached with adhesive to the left side of the CD changer unit.
- 2. Disconnect the card wire from connector UCW3 of the FL display and system control board on the back of the CD changer unit.
- 3. Disconnect the harness from connector RCW6 on the inner side of the main board in the body.
- 4. Remove the two screws **C** attaching the CD changer unit on the back of the body.
- 5. Remove the two screws **D** attaching the CD changer unit on the both side of the body.
- 6. Draw the CD changer unit upward from behind while pulling the rear panel outward.



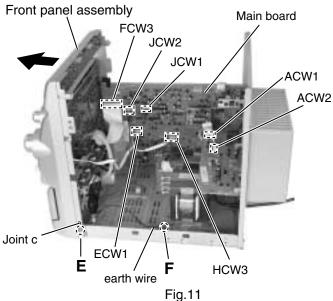
FL display & system Main board RCW6 control board Fig.8

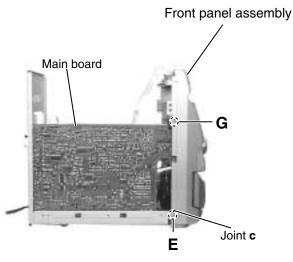




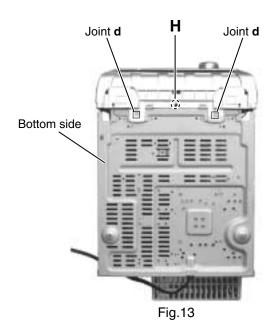
#### Removing the front panel assembly (See Fig.11 to 13)

- Prior to performing the following procedure, remove the metal cover and the CD changer unit.
- 1. Disconnect the card wire from connector FCW3 and the harness from connector ECW1,JCW1, JCW2 and HCW3 on the inner side of the main board in the body.
- 2. Remove the two screws **E** attaching the front panel assembly on both sides of the body.
- 3. Remove the screw **F** attaching the earth terminal extending from the cassette mechanism assembly.
- 4. Remove the screw **G** attaching the front panel assembly and main board.
- 5. Remove the screw **H** attaching the front panel assembly on the bottom of the body.
- Release the two joints c on both sides and two joints d on the bottom of the body using a screwdriver.









#### Removing the heat sink & Amp. board (See Fig.14 and 15)

- Prior to performing the following procedure, remove the metal cover and the CD changer unit.
- 1. Remove the four screws I attaching the heat sink cover on the back of the body. Remove the heat sink cover.
- 2. Remove the four screws **J** attaching the heat sink & Amp. board to the rear panel on the back of the body.
- 3. Remove the two screws **K** attaching the speaker terminal to the rear panel on the back of the body.
- 4. Disconnect the card wire from connector ACW1 & the harness from connector ACW2 on the Amp. board. (See Fig.11)
- 5. After moving the heat sink upward, remove the claws. Then pull out the heat sink & Amp. board inward.

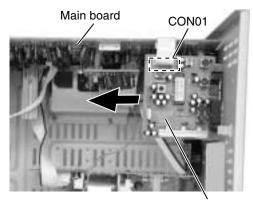
#### ■Removing the tuner pack (See Fig.15 to 16)

- Prior to performing the following procedure, remove the metal cover and CD changer unit.
- 1. Disconnect the card wire from connector CON01 on the tuner board.
- 2. Remove the two screws L attaching the tuner pack.

#### Removing the rear cover

(See Fig.17)

- Prior to performing the following procedure, remove the metal cover, CD changer unit, heat sink & Amp. board and tuner pack.
- 1. Remove the five screws **M**, and the screw **M**' attaching the rear panel.







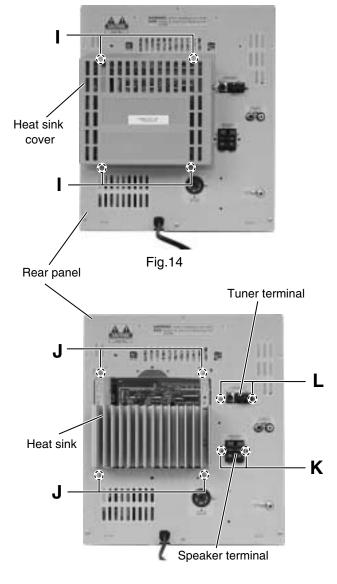
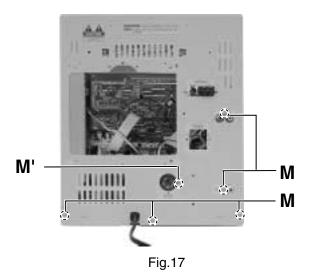


Fig.15

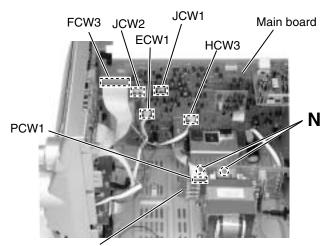


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#### Removing the main board

(See Fig. 18)

- · Prior to performing the following procedure, remove the metal cover. CD changer unit.
- 1. Disconnect the card wire from connector FCW3 and the harness from connector ECW1, JCW1, JCW2 and HCW3 on the main board.
- 2. Disconnect the harness from connector PCW1 on the power transformer board.
- 3. Remove the screw G attaching the main board holder. (See Fig.12)
- 4. Remove the two screws **N** attaching the heat sink and bottom chassis.



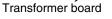
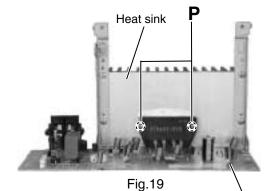
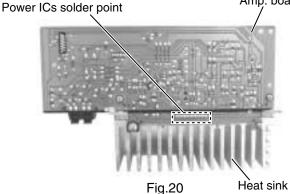


Fig.18





Amp. board



Power transformer PCW1 R R RCW2 Power cord Fig.21

#### Removing the power IC

(See Fig.19 and 20)

- · Prior to performing the following procedure, remove the metal cover CD changer unit and heat sink & Amp. board.
- 1. Remove the two screws P attaching the power IC to the heat sink.
- 2. Unsolder the power IC solder point.

#### Removing the power transformer (See Fig. 21)

- · Prior to performing the following procedure, remove the metal cover, heat sink & Amp board, tuner pack and rear cover.
- 1. Disconnect the power cord from connector RCW2 of the power transformer board.
- 2. Disconnect the harness from connector PCW1 of the power transformer board.
- 3. Remove the four screws R attaching the power transformer.

#### <Front panel assembly>

• Prior to performing the following procedure, remove the metal cover, the CD changer unit and the front panel assembly.

#### Removing the power / CD switch board (See Fig.22)

- 1. Disconnect the card wire from connector UCW1 on the power / CD switch board.
- 2. Remove the five screws **T** attaching the power / CD switch board and release the tab **e**.

# Removing the FL display & system control board

(See Fig. 22)

- 1. Disconnect the card wire from the connector UCW3, UJW5,UCW5 and UCW6 on the FL & System control board.
- 2. Remove the five screws **U** attaching the FL & System board.
- 3. Disconnect the card wire from the connector UCW2 on the FL & System control board.

#### ■Removing the front board (See Fig.23 to Fig.25)

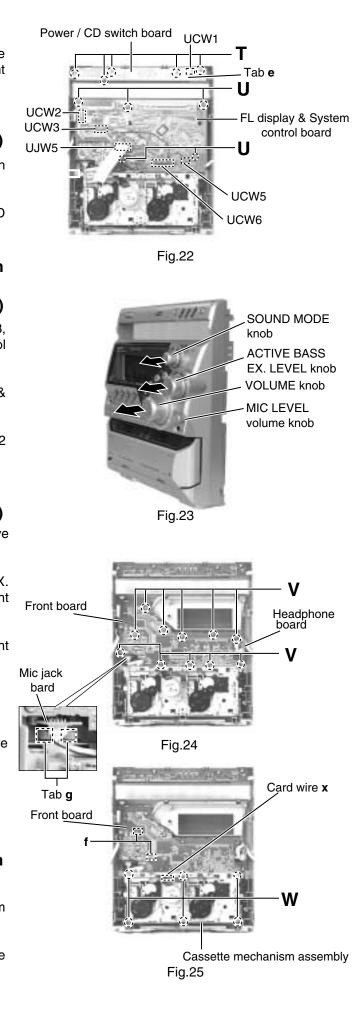
- Prior to performing the following procedure, remove the FL display & System control board.
- 1. Pull out the VOLUME knob, ACTIVE BASS EX. LEVEL knob and SOUND MODE knob from front side.
- 2. Remove the eleven screws **V** attaching the front board and release the two tabs **f** out ward.

# Removing the headphone board & Mic jack board (See Fig.24)

- Prior to performing the following procedure remove the FL display & System control board.
- 1. You can pull out the headphone board.
- 2. Remove the mic jack board and release the tab g.

# Removing the cassette mechanism assembly (See Fig.25)

- 1. Disconnect the card wire  $\mathbf{x}$  from the mechanism board on the cassette mechanism assembly.
- 2. Remove the six screws  ${\bf W}$  attaching the cassette mechanism assembly.



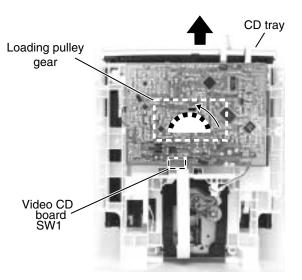
#### MX-K55V

#### <CD changer unit>

· Prior to performing the following procedure, remove the CD changer unit.

#### Removing the CD tray (See Fig.1 to 3)

- 1. Disconnect the card wire from connector SW1 of the video CD board.
- 2. Turn the biack loading pulley gear on the under side of the CD changer unit in the direction of the arrow and draw the CD tray toward the front until it stops.
- 3. Disconnect the card wire from connector CW6 of the Video CD board on the upper side of the CD changer unit.
- 4. Push down the two tray stoppers marked **a** and pull out the CD tray.





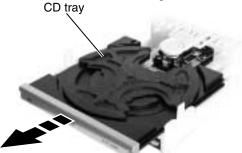
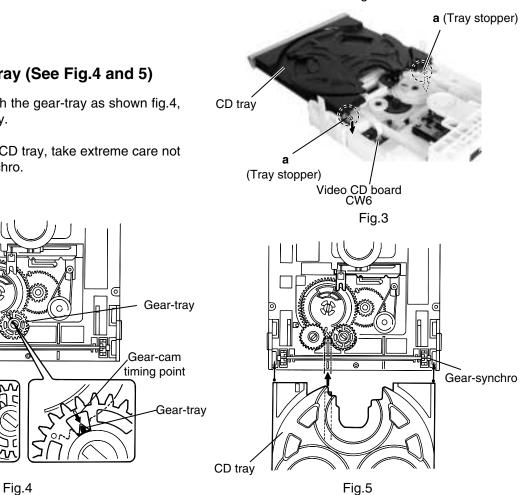


Fig.2



#### ■ Reinstall the CD tray (See Fig.4 and 5)

- 1. Align the gear-cam with the gear-tray as shown fig.4, then mount the CD tray.
- 2. When assembling the CD tray, take extreme care not engage with gear-synchro.

Gear-cam

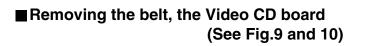
Gear-convert

Gear-convert

Gear-tray

# Removing the sensor board / the turn table motor assembly (See Fig.6 to 8)

- Prior to performing the following procedure, remove the CD tray.
- 1. Remove the screw **A** attaching the sensor board and release the two tabs **b** attaching the sensor board on the under side of the CD tray.
- 2. Disconnect the harness from connector CW1 on the sensor board and release the harness from the two hooks **c**. Remove the sensor board.
- 3. Remove the screw **B** attaching the turn table. Detach the turn table from the tray.
- 4. Pull outward the tab marked **d** attaching the turn table motor assembly on the upper side of the tray and detach the turn table motor assembly from the tray.



- Prior to performing the following procedure, remove the CD tray.
- 1. Disconnect the harness from connector on the CD mechanism board in the CD mechanism assembly on the under side of the CD changer unit. Disconnect the card wire from the pickup unit connector.
- 2. Detach the belt from the pulley on the upper side of the CD changer unit (Do not stain the belt with grease).
- 3. Disconnect the card wire from the connector SW1 on the Video CD board.
- ※ Remove the three screws D attaching the video CD board. First release the three tabs f and tabs e attaching the video CD board motor to raise the video CD board slightly, then release the video CD board.

If the tabs **e** and **f** are hard to release, it is recommendable to unsolder the two soldered points on the motor terminal of the video CD board.

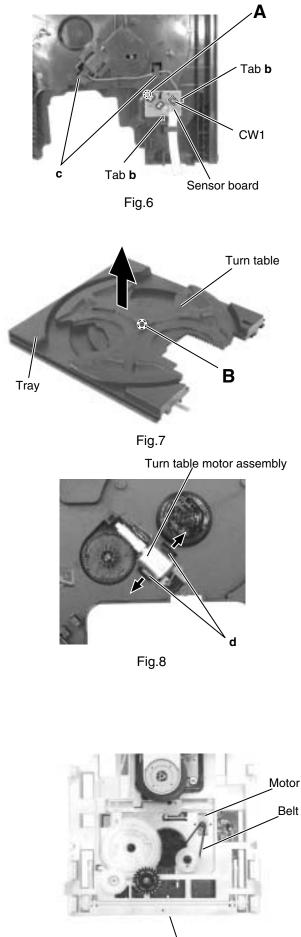


Fig.9 CD changer unit

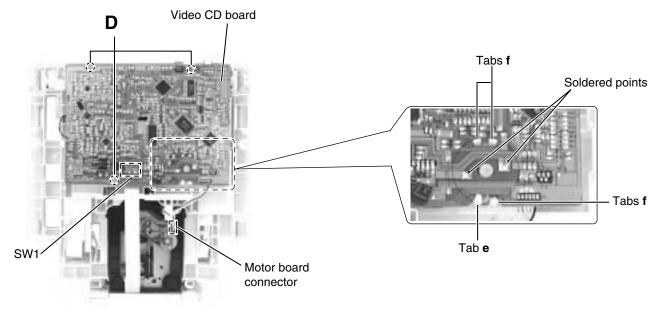
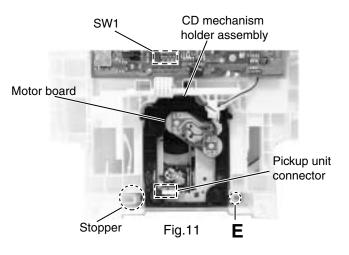


Fig.10

#### Removing the CD mechanism holder assembly (mechanism included) (See Fig.11 to 13)

- 1. Disconnect the card wire from pickup unit connector on the motor board in the CD mechanism holder assembly on the under side of the CD changer unit.
- 2. Remove the screw **E** attaching the shaft on the right side of the CD mechanism holder assembly.
- Pull outward the stopper fixing the shaft on the left side and remove the CD mechanism holder assembly from behind in the direction of the arrow ★.
- 4. Pull out the CD mechanism holder assembly.



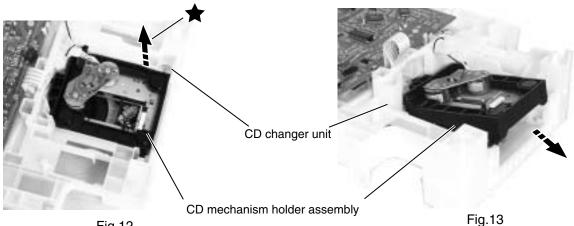


Fig.12

#### <Cassette mechanism section>

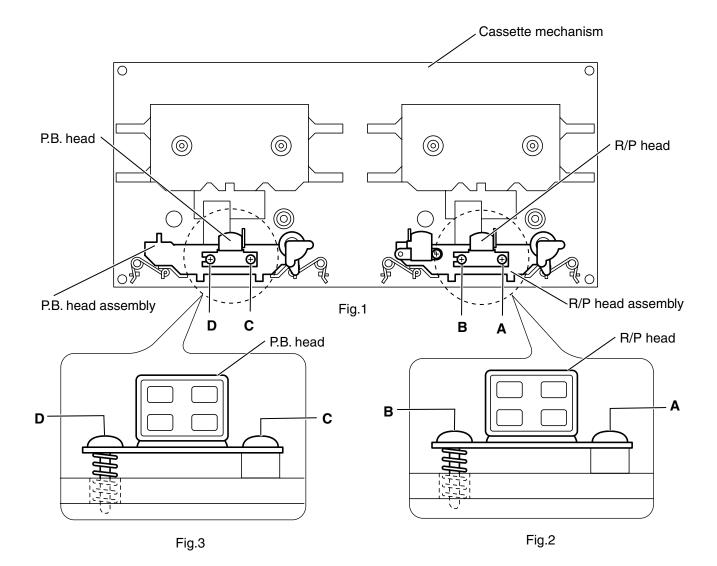
• Prior to performing the following procedure, removing the cassette mechanism.

#### ■ Removing the R/P head. (Fig.1 to 3)

- 1. Remove the screw **A** attaching the R/P head right side.
- 2. Remove the screw **B** attaching R/P head left side. (Screw **B** : Head azimuth adjusting screw.)

#### ■ Removing the P.B. head. (Fig.1 to 3)

- 1. Removing the screw **C** attaching the P.B head right side.
- 2. Removing the screw **D** attaching the P.B head left side. (Screw **D** : Head azimuth adjusting screw.)



#### MX-K55V

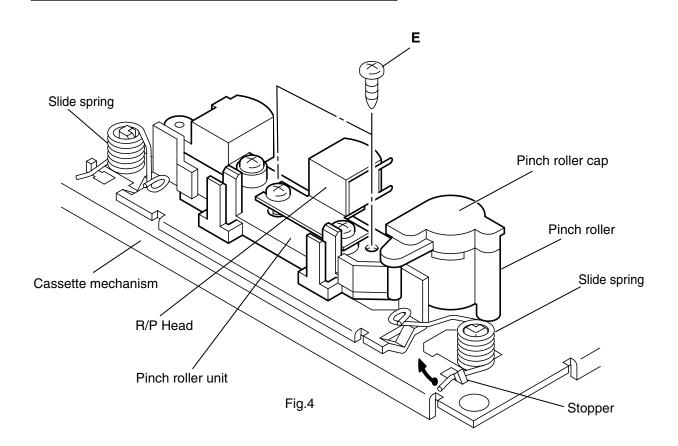
Removing the pinch roller unit.

(Fig. 4)

- Prior to performing the following procedure, removing the cassette mechanism.
- 1. Remove the two screws **E** attaching the pinch roller unit.

Attention:

The pinch roller cap is forcefully fitted to the shaft of the pinch roller unit. If the pinch roller cap is taken out by force, the shaft will be broken. When replacing the pinch roller, it should be changed as a pinch roller unit itself.



#### Removing the flywheel. (Fig.5 to 7)

- Prior to performing the following procedure, removing the cassette mechanism.
- 1. Remove the cut washers at **a** and **b** from the capstan shaft. Then remove the flywheel. When reassembling the flywheel, be sure to use new cut washers as they cannot be reused.

#### Removing the motor. (Fig.7 to 9)

- Prior to performing the following procedure, removing the cassette mechanism.
- 1. Unsolder the solder point on the motor terminal.
- 2. Remove the capstan belt from the motor pulley.
- 3. Remove the two screws F attaching the motor bracket.

Motor bracket

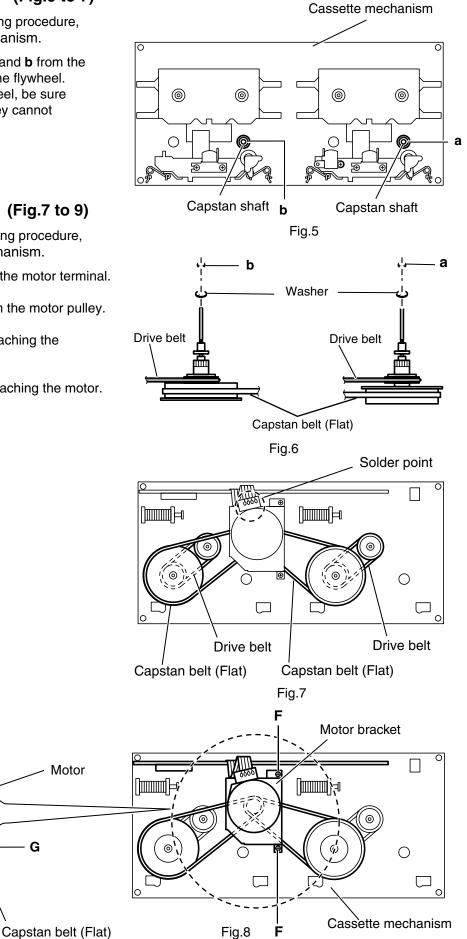
Capstan belt (Flat)

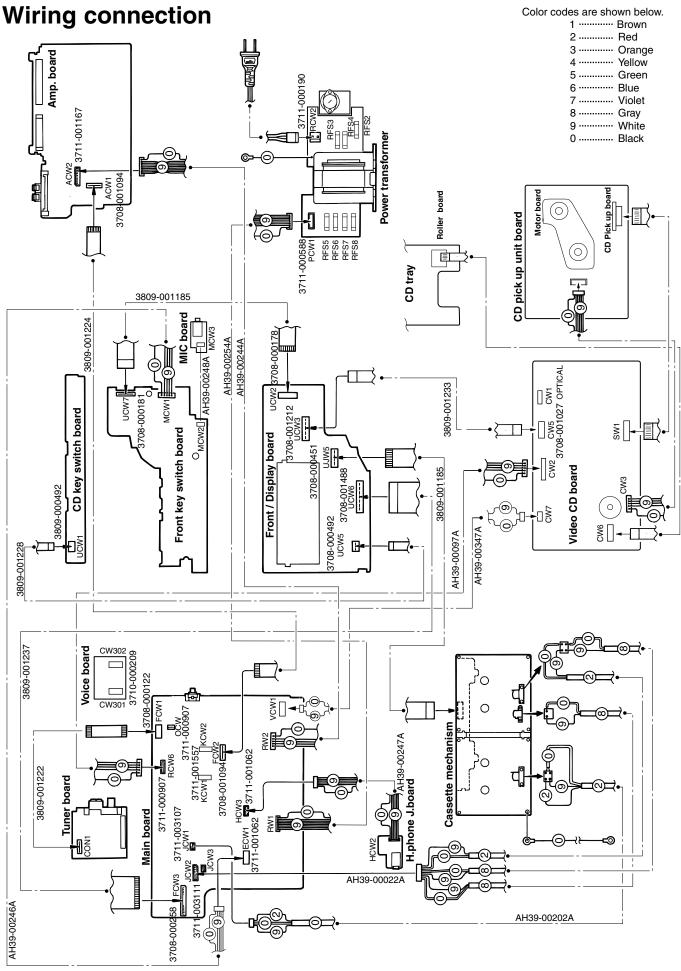
Fig.9

G

4. Remove the two screws G attaching the motor.

G





# Adjustment method

1. Tuner

$\begin{array}{c c c c c c c c c c c c c c c c c c c $	
	_

\* Adjustment Location of Tuner board

ITEAM	AM(MW) OSC Adjustment	AM(MW) RF Adjustment	LW OSC Adjustment (Except for J/C)	AM(MW) RF Adjustment
Received FREQ.	531~1602 KHz (9kHz step) 530~1600 KHz (10kHz step)	594 KHz	146~290 KHz	150 KHz
Adjustment point	MO	MA	LO	LA
Output	$1 \sim 7.0 \pm 0.5 V$	Maximum Output(Fig1-4)	2~7.0 ±0.5 V	Maximum Output(Fig1-4)

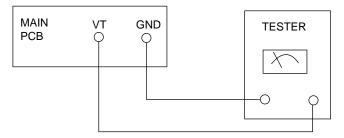


Fig 1-4 OSC Voltage

#### MX-K55V

FM	FM THD Adjustment			
SSG FREQ.	98 MHz			
Adjustment point (FM DET)	FM DETECTOR COIL			
Output	60 dB			
Minimum Disto (Figure 1-1)	rtion (0.4% below)			

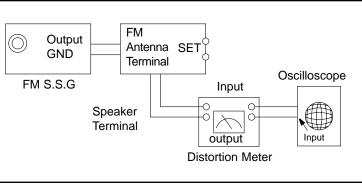


Figure1-1 IF CENTER and THD Adjustment

98 MHz		
AdjustmentBEACONpointSENSITIVITY(SVR1)SEMI-VR(20KΩ)		
28 dB( ± 2dB)		
Adjust SVR1 so that "TUNED" of FL T is lighted (Figure 1-2)		

\*Adjust FM S.S.G level to 28dB

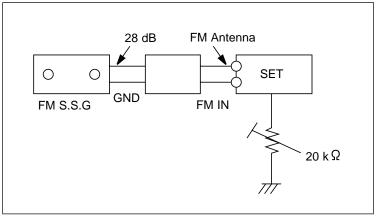


Figure1-2 FM Auto Search Level Adjustment

AM(MW) I.F Adjustment		
SSG FREQ.	450 kHz	
Frequency	531 kHz (9kHz step) 530 kHz (10kHz step)	
Adjustment point	AM IF	
Maximum output (Figure 1-3)		

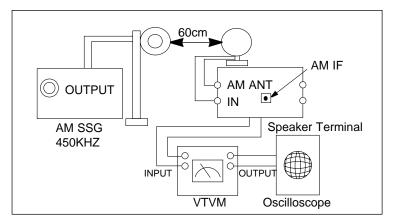


Figure1-3 AM I.F Adjustment

#### 2 Cassette Deck

#### To adjust tape speed

Notes 1) Measuring tape: i) VT-712 (Tapes recorded with 3kHz) ii) AC-225 2) Connect the cassette deck to the frequency counter as in figure 1-5.

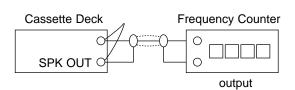
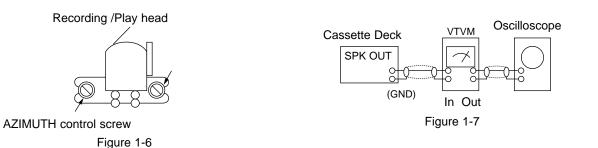


Figure 1-5

Step	ltem	Pre-Setup Condition	Pre-Setup	To Adjust	Standard	Remark
1	NOR SPEED Control	OUT (connected to the frequency counter)	<ol> <li>Deck 1:VT-712</li> <li>Press PLAY SW button</li> <li>Deck 2:Same as above</li> </ol>	Turn VSR1 to left and right (FRONT board)	3KHz	±1% range



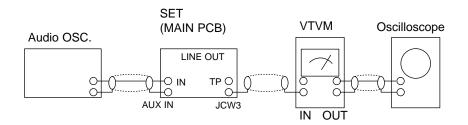


Figure 1-8

#### To adjust playback level/REC

Notes
 Before the actual adjustment, clean the play/recording head.
 Measuring tape :

 i) VT-703 (10kHz AZIMUTH control)
 ii) AC-225

 The cassette deck is connections as shown in figure 1-7.

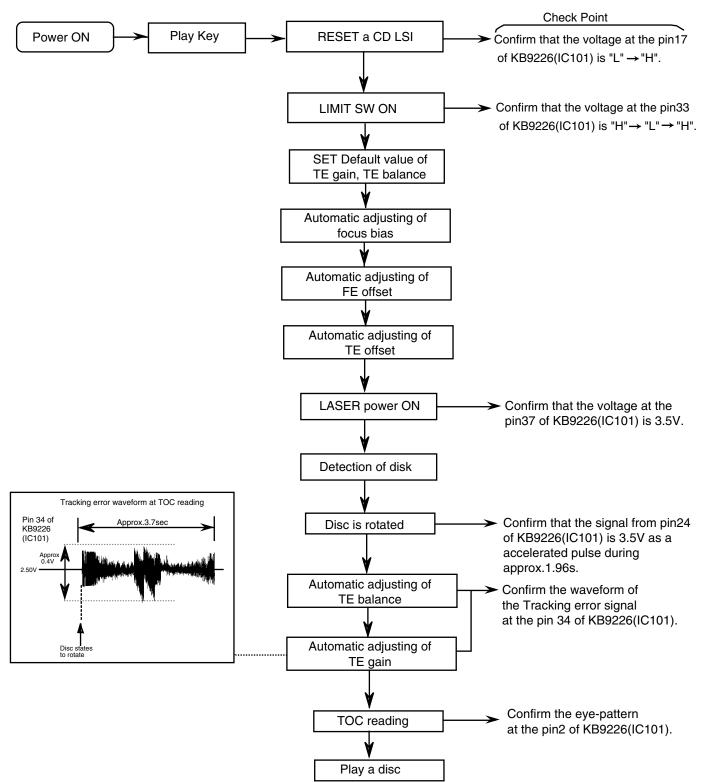
#### 1. Adjust Deck A Play Level

Step	ltem	Pre-Setup Condition	Pre-Setup	To Adjust	Standard	Remark
1	AZIMUTH	SPK OUT (VTVM is connected to the scope)	After putting VT - 703 into Deck A - Press FWD PLAY button.	Turn the control screw to as shown in Figure 1-6.	Max output and same phase (both channels)	After adjustment secure it with REGION LOCK.

#### 2. Adjust Deck B Play Level/REC BIAS

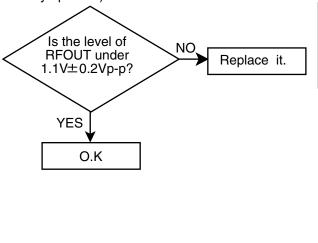
Step	ltem	Pre-Setup Condition	Pre-Setup	To Adjust	Standard	Remark
1	AZIMUTH	SPK OUT (VTVM is connected to the scope)	After putting VT-703 into Deck B 1)Press FWD PLAY button.	Turn the control screw to as shown in Figure 1-6.	Max output and same phase (both channels)	After adjustment secure it with REGION LOCK.
2	Recording Bias Voltage	Fig 1-8	After putting AC-225 into Deck B 1)Press REC PLAY button. 2)MAIN PCB JCW3, connected to VTVM	Turn JSR2L,JSR2R to the right and left	7mV(±0.5mV)	

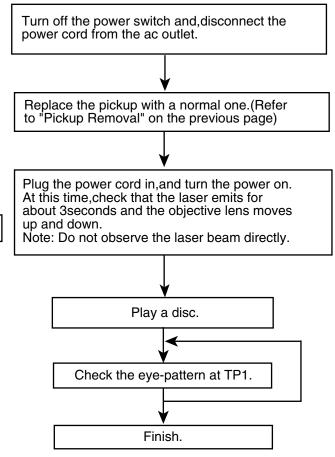
# Flow of functional operation until TOC read



### Maintenance of laser pickup

- Cleaning the pick up lens Before you replace the pick up, please try to clean the lens with a alcohol soaked cotton swab.
- (2) Life of the laser diode When the life of the laser diode has expired, the following symptoms will appear.
  - 1. The level of RF output (EFM output:ampli tude of eye pattern) will below.





(3) Semi-fixed resistor on the APC PC board

The semi-fixed resistor on the APC printed circuit board which is attached to the pickup is used to adjust the laser power. Since this adjustment should be performed to match the characteristics of the whole optical block, do not touch the semi-fixed resistor.

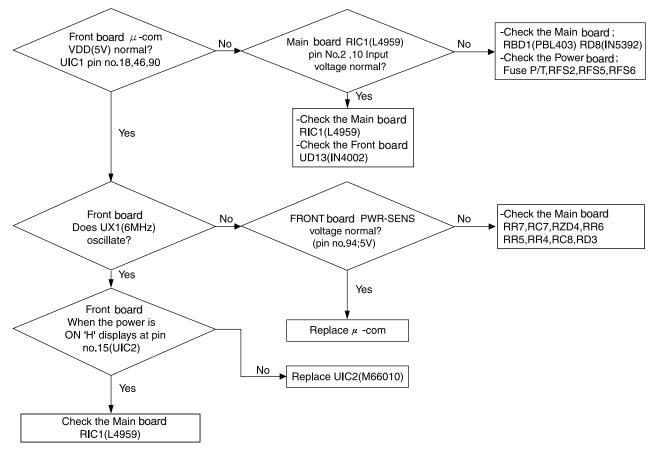
If the laser power is lower than the specified value, the laser diode is almost worn out, and the laser pickup should be replaced.

If the semi-fixed resistor is adjusted while the pickup is functioning normally, the laser pickup may be damaged due to excessive current.

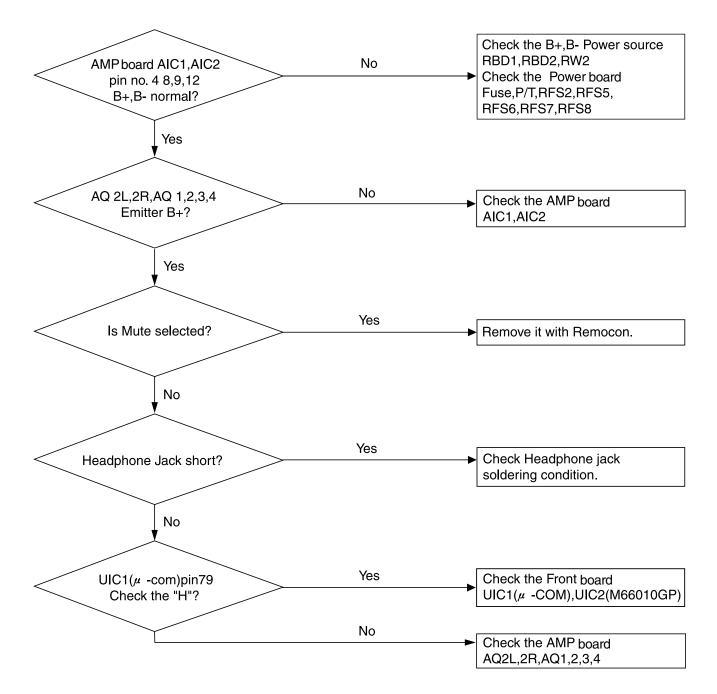
# Troubleshooting

### **1.Amplifier**

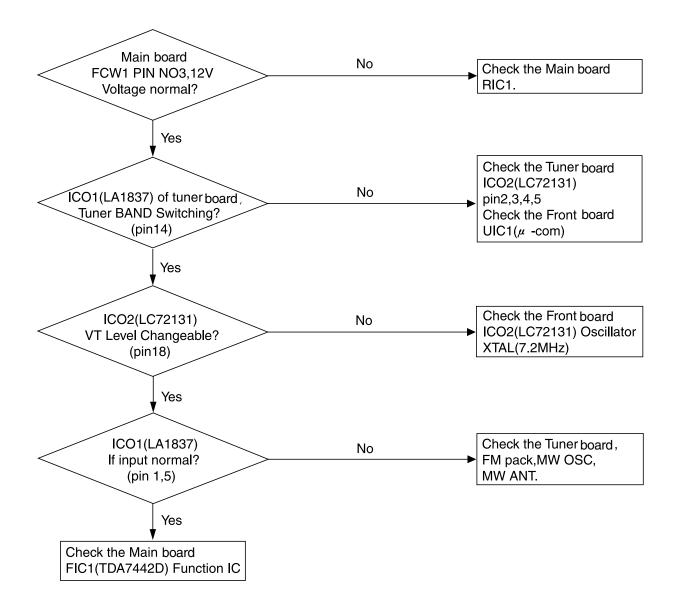
#### **Power Malfunction**



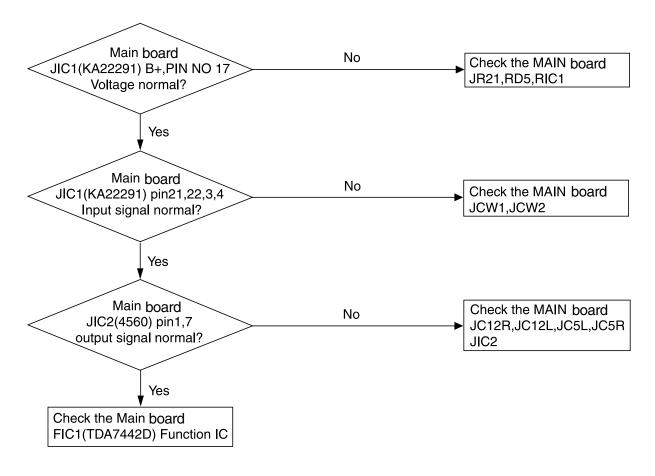
#### <No Output>



#### 2. Tuner malfunction (FM/AM)

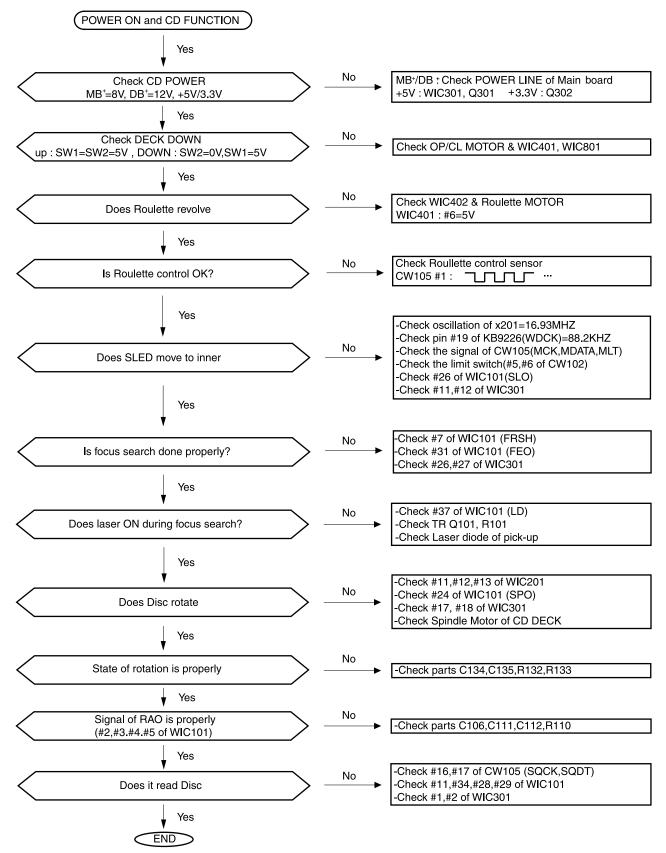


#### 3. Tape



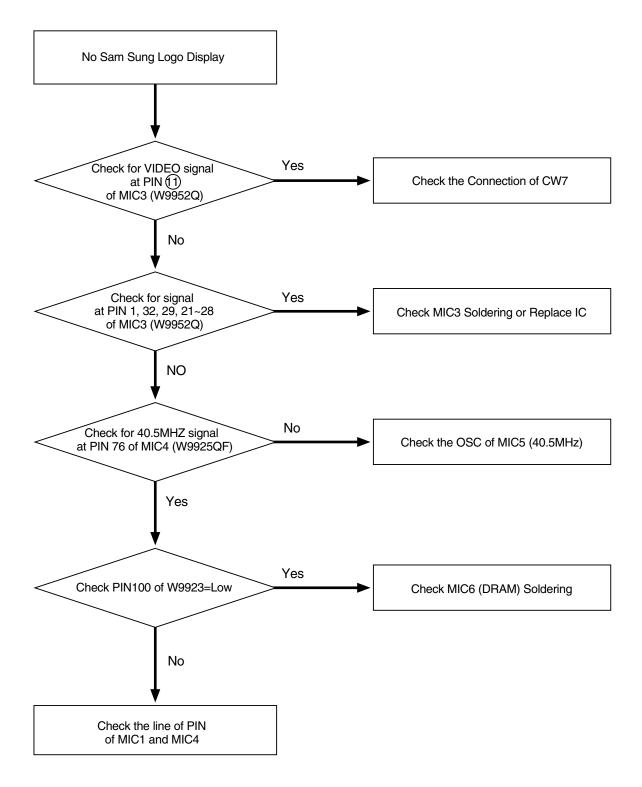
#### 4. Video CD

#### < No DISC>



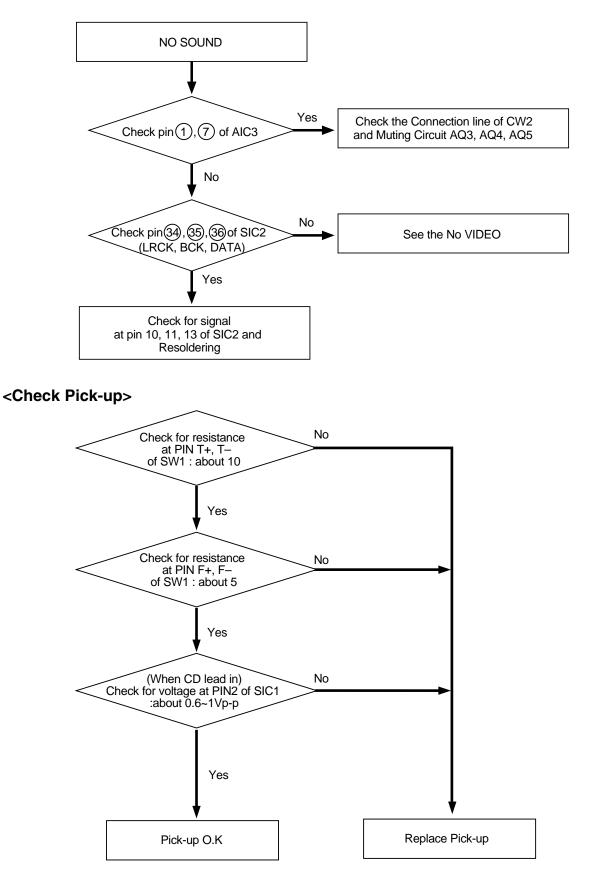
#### <No VIDEO>

• Check the Voltage (+5V, +3.3V)

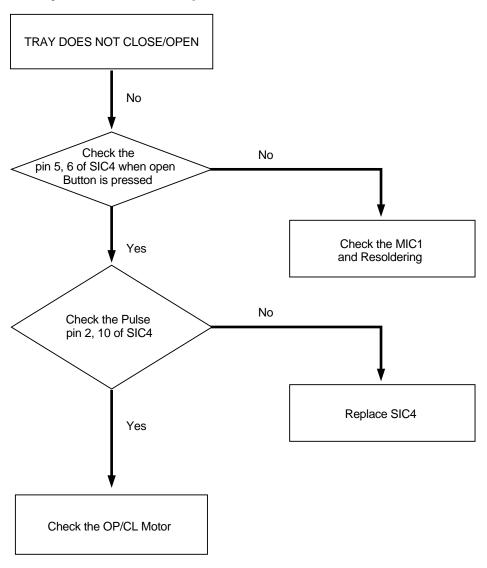


#### <No sound of CD Play>

- Check 16.9344MHz OSC at pin38 of MIC1
- Check Voltage (+5, ±12)
- Check all Connection between VCD pack board and Main, Front board



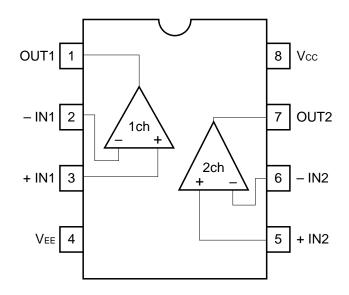
#### <3CD Tray does not close/open>



### **Description of major ICs**

■ BA4560 (FIC2,FIC4,HIC1, JIC2,UIC3) : Dual op. amp.

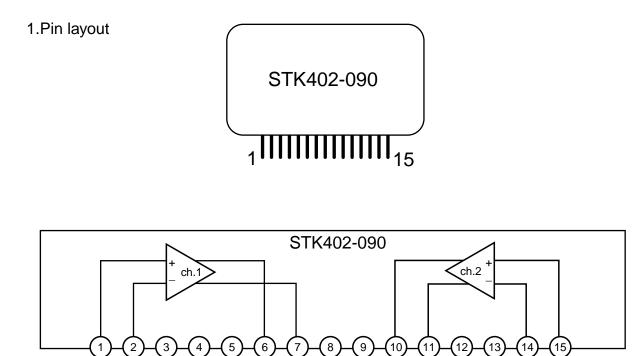
#### 1. Pin layout



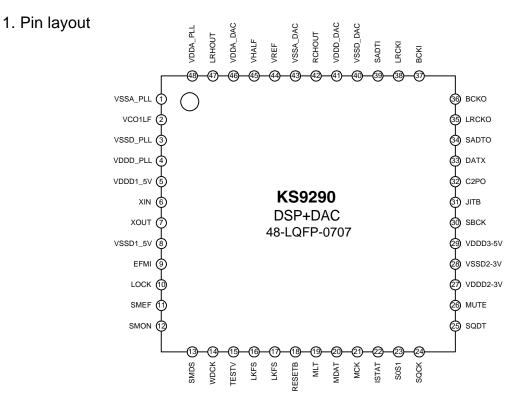
**STK402-090 (AIC1) : Power amp.** 

CH1

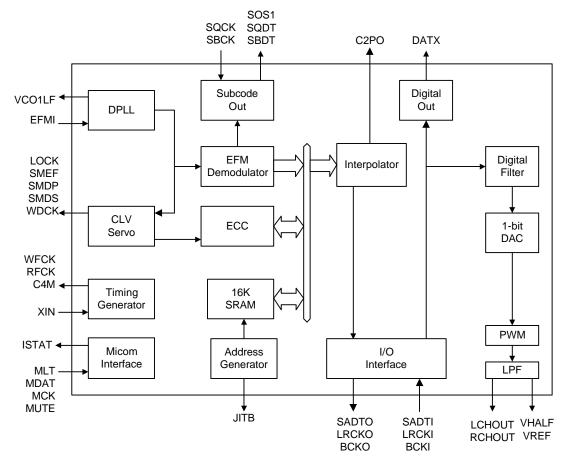
IN



#### KS9290 (IC201) : Digital signal processor for CD player



#### 2. Block diagram

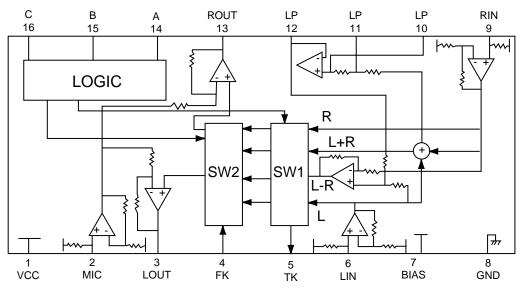


#### 3. Pin function

Pin. No.         Symbol         Type         Function           1         VSSA_PLL         -         Analog Ground for DPLL           2         VCO1LF         O         Pump out for VCO1           3         VSSD_PLL         -         Digital Ground Separated Bulk Bias for DPLL (3V Power)           5         VDDD1-SV         -         Digital Power (SV Power, I/O PAD)           6         XIN         I         X'tal oscillator output           7         XOUT         O         X'tal oscillator output           8         VSSD1         -         Digital Ground (I/O PAD)           9         EFMI         I         EFM secontral output for Spindle Motor drive           10         LOCK         O         CLV Servo locking status output           11         SMEP         O         LPF time constant control of the Motor drive           14         WDCK         O         Word clock output (Normal Speed: 88.2KHz, Double Speed: 176.4KHz)           15         TESTV         I         Various Data/Clock Input           16         LKFS         O         The Lock status output of frame sync           17         C4M         O         4.2336MHz clock input           18         RESETB         I         Syst	3. Pin fur	nction		KS9290
2         VC01LF         0         Pump out for VC01           3         VSSD_PLL         Digital Ground Separated Bulk Bias for DPLL (3V Power)           5         VDDD PLL         Digital Power (SV Power, I/O PAD)           6         XIN         I         Xtal oscillator output (16.9344MHz)           7         XOUT         O         Xtal oscillator output           8         VSSD1         Digital Ground (I/O PAD)           9         EFMI         I         EFM signal input           10         LOCK         O         CLV Servo locking status output           11         SMEF         O         LPre time constant control of the spindle servo error signal           12         SMDP         O         Phase control output for Spindle Motor drive           13         SMDS         O         Speed control output for Spindle Motor drive           14         WDCK         O         Word clock output for Spindle Motor drive           15         TESTV         I         Various Data/Clock Input           16         LKFS         O         The Lock status output for Micom           21         MCK         I         Serial data receiving clock input form Micom           22         ISTAT         O         The internal status outp	Pin.No.	Symbol	Туре	Function
3       VSSD_PLL       -       Digital Ground Separated Bulk Bias for DPLL         4       VDDD_FLL       -       Digital Power (SV Power, I/O PAD)         5       VDD1-5V       Digital Fower (SV Power, I/O PAD)         6       XIN       1       Xtal oscillator input (16.9344MHz)         7       XOUT       O       Xtal oscillator output         8       VSSD1       Digital Ground (I/O PAD)         9       EFMI       1       EFM signal input         10       LOCK       O       CLV Servo locking status output         11       SMEF       O       LPF time constant control of the spindle servo error signal         12       SMDP       O       Phase control output for Spindle Motor drive         13       SMDS       O       Speed control output for Spindle Motor drive         14       WDCK       O       Word clock output for Spindle Motor drive         15       TESTV       I       Various Data/Clock Input         16       LKFS       O       The Lock status output of frame sync         17       C4M       O       4.2336MHz clock output         18       RESETB       I       System Reset at 'L'         19       MLT       I       Latch signal input from	1	VSSA_PLL	-	Analog Ground for DPLL
4       VDDD_PLL       -       Digital Power (SV Power, I/O PAD)         5       VDD1-SV       -       Digital Power (SV Power, I/O PAD)         6       XIN       1       Xtal oscillator output (16.334MHz)         7       XOUT       O       Xtal oscillator output (16.944MHz)         8       VSSD1       -       Digital Ground (I/O PAD)         9       EFMI       I       EFM signal input         10       LOCK       O       CLV Servo locking status output         11       SMEF       O       LPF time constant control of the spindle servo error signal         12       SMDP       O       Phase control output for Spindle Motor drive         13       SMDS       O       Speed control output for Spindle Motor drive         14       WDCK       O       Vord clock output (Normal Speed : 88.2KHz, Double Speed : 176.4KHz)         15       TESTV       I       Various Data/Clock output         16       LKFS       O       The Lock status output for firme sync         17       C4M       0       4.2330MHz clock output         18       RESETB       I       System Reset at 'L'         19       MLT       I       Latch signal input from Micom         22       ISTA	2	VCO1LF	0	Pump out for VCO1
5     VDDD1-5V     -     Digital Power (5V Power, I/O PAD)       6     XIN     1     X'tal oscillator output       7     XOUT     O     X'tal oscillator output       8     VSSD1     -     Digital Ground (I/O PAD)       9     EFMI     1     EFM signal input       10     LOCK     O     CLV Servo locking status output       11     SMEF     O     LPF time constant control of the spindle servo error signal       12     SMDP     O     Phase control output for Spindle Motor drive       13     SMDS     O     Speed control output for Spindle Motor drive       14     WDCK     O     Word clock output (Normal Speed : 88.2KHz, Double Speed : 176.4KHz)       15     TESTV     I     Various Data/Clock Input       16     LKFS     O     The Lock status output of frame sync       17     C4M     O     4.2336MHz clock output from Micom       20     MDAT     I     Serial data input from Micom       21     MCK     I     Serial data receiving clock input from Micom       22     ISTAT     O     The internal status output to Micom       23     SOS1     O     Sub code-Q data rensferring bit clock input       24     SOCK     I     Sub code-Q data serial output <tr< td=""><td>3</td><td>VSSD_PLL</td><td>-</td><td>Digital Ground Separated Bulk Bias for DPLL</td></tr<>	3	VSSD_PLL	-	Digital Ground Separated Bulk Bias for DPLL
6       XIN       I       X'tal oscillator input (16.9344MHz)         7       XOUT       O       X'tal oscillator output         8       VSSD1       Digital Ground (I/O PAD)         9       EFMI       I       EFM signal input         10       LOCK       O       CLV Servo locking status output         11       SMEF       O       LPF time constant control of the spindle servo error signal         12       SMDP       O       Phase control output for Spindle Motor drive         13       SMDS       O       Speed control output for Spindle Motor drive         14       WDCK       O       The Lock status output of frame sync         17       C4M       O       4.239MHz clock output         18       RESETB       I       System Reset at 'L'         19       MLT       I       Latch signal input from Micom         21       MCK       I       Serial data receiving clock input from Micom         22       ISTAT       O       The internal status output to Micom         23       SOS1       O       Sub code-Q data serial output         24       SQCK       I       Sub code-Q data serial output         25       SQDT       O       Sub code-Q data serial	4	VDDD_PLL	-	Digital Power Separated Bulk Bias for DPLL (3V Power)
7       XOUT       O       X'tal oscillator output         8       VSSD1       -       Digital Ground (I/O PAD)         9       EFMI       1       FFM signal input         10       LOCK       O       CLV Servo locking status output         11       SMEF       O       LPF time constant control of the spindle servo error signal         12       SMDP       O       Phase control output for Spindle Motor drive         13       SMDS       O       Speed control output for Spindle Motor drive         14       WDCK       O       Word dock output (Normal Speed : 82.KHz, Double Speed : 176.4KHz)         15       TESTV       I       Various Data/Clock Input         16       LKFS       O       The Lock status output of frame sync         17       C4M       O       4.2336MHz clock output         18       RESETB       I       System Reset at 'L'         19       MLT       1       Latch signal input from Micom         21       MCK       1       Serial data receiving clock input from Micom         22       ISTAT       O       Sub code-Q data transferring bit clock input         24       SOCK       1       Sub code-Q data serial output         27       VDDD2	5	VDDD1-5V	-	Digital Power (5V Power, I/O PAD)
8         VSSD1         -         Digital Ground (I/O PAD)           9         EFMI         I         EFM signal input           10         LOCK         O         CLV Servo locking status output           11         SMEF         O         LPF time constant control of the spindle Motor drive           13         SMDS         O         Speed control output for Spindle Motor drive           14         WDCK         O         Word clock output (Normal Speed : 86.2KHz, Double Speed : 176.4KHz)           15         TESTV         I         Various Data/Clock Input           16         LKFS         O         The Lock status output of frame sync           17         C4M         Q         4.2336MHz clock output           18         RESETB         I         System Reset at 'L'           19         MLT         I         Latch signal input from Micom           20         MDAT         I         Serial data input from Micom           21         MCK         I         Serial data input from Micom           22         ISTAT         O         The internal status output for Micom           23         S0S1         O         Sub code-Q data transferring bit clock input           24         SQCK         I	6	XIN	I	X'tal oscillator input (16.9344MHz)
9       EFMI       I       EFM signal input         10       LOCK       O       CLV Servo locking status output         11       SMEF       O       LPF time constant control of the spindle servo error signal         12       SMDP       O       Phase control output for Spindle Motor drive         13       SMDS       O       Speed control output for Spindle Motor drive         14       WDCK       O       Word clock output (Normal Speed : 88.2KHz, Double Speed : 176.4KHz)         15       TESTV       I       Various Data/Clock Input         16       LKFS       O       The Lock status output of frame sync         17       C4M       O       4.2336MHz clock output         18       RESETB       I       System Reset at 'L'         19       MLT       I       Latch signal input from Micom         21       MCK       I       Serial data receiving clock input from Micom         22       ISTAT       O       The internal status output to Micom         23       SQS1       O       Sub code-Q data transferring bit clock input         24       SQCK       I       Sub code-Q data serial output         25       SQDT       O       Sub code data transferring bit clock	7	XOUT	0	X'tal oscillator output
10       LOCK       O       CLV Servo locking status output         11       SMEF       O       LPF time constant control of the spindle servo error signal         12       SMDP       O       Phase control output for Spindle Motor drive         13       SMDS       O       Speed control output for Spindle Motor drive         14       WDCK       O       Word clock output (Normal Speed : 86.2KHz, Double Speed : 176.4KHz)         15       TESTV       I       Various Data/Clock Input         16       LKFS       O       The Lock status output of frame sync         17       C4M       O       4.2336MHz clock output         18       RESETB       I       System Reset at 'L'         19       MLT       I       Latch signal input from Micom         20       MDAT       I       Serial data input from Micom         21       MCK       I       Serial data receiving clock input from Micom         22       ISTAT       O       The internal status output to Micom         23       SOS1       O       Sub code-Q data transferring bit clock input         24       SQCK       I       Sub code and transferring bit clock input         25       SQDT       O       Sub code and transferring bit clock input<	8	VSSD1	-	Digital Ground (I/O PAD)
11       SMEF       O       LPF time constant control of the spindle servo error signal         12       SMDP       O       Phase control output for Spindle Motor drive         13       SMDS       O       Speed control output for Spindle Motor drive         14       WDCK       O       Word clock output (Normal Speed : 88.2KHz, Double Speed : 176.4KHz)         15       TESTV       I       Various Data/Clock Input         16       LKFS       O       The Lock status output of frame sync         17       C4M       O       4.2336MHz clock output         18       RESETB       I       System Reset at 'L'         19       MLT       I       Latch signal input from Micom         20       MDAT       I       Serial data input from Micom         21       MCK       I       Sub code sync signal (S0-K1) output         23       SOS1       O       Sub code-Q data ransferring bit clock input         24       SQCK       I       Sub code-Q data ransferring bit clock input         25       SQDT       O       Sub code sync signal (S0+S1) output         26       MUTE       I       System mute at 'H'         27       VDDD2-3V       -       Digital Power (5V Power, I/O PAD)	9	EFMI	I	EFM signal input
12       SMDP       O       Phase control output for Spindle Motor drive         13       SMDS       O       Speed control output for Spindle Motor drive         14       WDCK       O       Word clock output (Normal Speed : 88.2KHz, Double Speed : 176.4KHz)         15       TESTV       I       Various Data/Clock Input         16       LKFS       O       The Lock status output of frame sync         17       C4M       O       4.2336MHz clock output         18       RESETB       I       System Reset at 'L'         19       MLT       I       Latch signal input from Micom         20       MDAT       I       Serial data input from Micom         21       INCK       I       Serial data receiving clock input from Micom         22       ISTAT       O       The internal status output to Micom         23       S0S1       O       Sub code-Q data transferring bit clock input         26       MUTE       I       System mute at 'H'         27       VDD2-3V       Digital Power (3V Power, Internal Logic)         28       VSD2       -       Digital Cround (Internal Logic)         28       VDD3-5V       -       Digital audio data output         34       JATX	10	LOCK	0	CLV Servo locking status output
13       SMDS       O       Speed control output for Spindle Motor drive         14       WDCK       O       Word clock output (Normal Speed : 88.2KHz, Double Speed : 176.4KHz)         15       TESTV       I       Various Data/Clock Input         16       LKFS       O       The Lock status output of frame sync         17       C4M       O       4.2336MHz clock output         18       RESETB       I       System Reset at 'L'         19       MLT       I       Latch signal input from Micom         20       MDAT       I       Serial data receiving clock input from Micom         21       MCK       I       Serial data receiving clock input from Micom         23       S0S1       O       Sub code synce signal (S0+S1) output         24       SQCK       I       Sub code synce signal (S0+S1) output         25       SQDT       O       Sub code synce signal (S0+S1) output         26       MUTE       I       System mute at 'H'         27       VDDD2-3V       Digital Power (SV Power, Internal Logic)         28       VSSD2       Digital Power (SV Power, I/O PAD)         30       SBCK       I       Sub code supt         32       C2PO       O       C2 point	11	SMEF	0	LPF time constant control of the spindle servo error signal
14       WDCK       O       Word clock output (Normal Speed : 88.2KHz, Double Speed : 176.4KHz)         15       TESTV       I       Various Data/Clock Input         16       LKFS       O       The Lock status output of frame sync         17       C4M       O       4.2336MHz clock output         18       RESETB       I       System Reset at 'L'         19       MLT       I       Latch signal input from Micom         20       MDAT       I       Serial data input from Micom         21       MCK       I       Serial data receiving clock input from Micom         22       ISTAT       O       The internal status output to Micom         23       S0S1       O       Sub code-Q data transferring bit clock input         24       SQCK       I       Sub code-Q data serial output         25       SQDT       O       Sub code-Q data serial output         26       MUTE       I       System mute at 'H'         27       VDD03-5V       Digital Power (5V Power, I/O PAD)         30       SBCK       I       Sub code data transferring bit clock         31       JITB       O       Internal SRAM jitter margin status output         32       C2PO       O <t< td=""><td>12</td><td>SMDP</td><td>0</td><td>Phase control output for Spindle Motor drive</td></t<>	12	SMDP	0	Phase control output for Spindle Motor drive
15       TESTV       I       Various Data/Clock Input         16       LKFS       O       The Lock status output of frame sync         17       C4M       O       4.2336MHz clock output         18       RESETB       I       System Reset at 'L'         19       MLT       I       Latch signal input from Micom         20       MDAT       I       Serial data receiving clock input from Micom         21       MCK       I       Serial data receiving clock input from Micom         23       S0S1       O       Sub code sync signal (S0+S1) output         24       SQCK       I       Sub code-Q data serial output         25       SQDT       O       Sub code-Q data serial output         26       MUTE       I       System mute at 'H'         27       VDDD2-3V       Digital Power (3V Power, Internal Logic)         28       VDD3-5V       -       Digital Power (5V Power, I/O PAD)         30       SBCK       I       Sub code data transferring bit clock         31       JITB       O       Internal SRAM jitter margin status output         32       C2PO       C2 pointer output       Gata output         33       DATX       O       Digital audio data outpu	13	SMDS	0	Speed control output for Spindle Motor drive
16LKFSOThe Lock status output of frame sync17C4MO4.2336MHz clock output18RESETBISystem Reset at 'L'19MLTILatch signal input from Micom20MDATISerial data input from Micom21MCKISerial data receiving clock input from Micom22ISTATOThe internal status output to Micom23S0S1OSub code-Q data transferring bit clock input24SQCKISub code-Q data serial output25SQDTOSub code-Q data serial output26MUTEISystem mute at 'H'27VDD2-3VDigital Power (3V Power, Internal Logic)28VSSD2-Digital Power (6V Power, I/O PAD)30SBCKISub code data transferring bit clock31JITBOInternal SRAM jitter margin status output33DATXODigital audio data output34SADTOOSerial audio data output (48 slot, MSB first)35LRCKOOChannel clock output36BCKIIBit clock input37BCKIIBit clock input38LRCKIIChannel clock input39SADTIISerial audio data input (48 slot, MSB first)40VSSD_DAC-Digital Power for DAC (3V Power)41VDD_DAG-Digital Power for DAC (3V Power)42RCHOUTOReference V	14	WDCK	0	Word clock output (Normal Speed : 88.2KHz, Double Speed : 176.4KHz)
17C 4MO4.2336MHz clock output18RESETBISystem Reset at 'L'19MLTILatch signal input from Micom20MDATISerial data input from Micom21MCKISerial data receiving clock input from Micom22ISTATOThe internal status output to Micom23S0S1OSub code sync signal (S0+S1) output24SQCKISub code-Q data transferring bit clock input25SQDTOSub code-Q data serial output26MUTEISystem mute at 'H'27VDDD2-3VDigital Power (3V Power, Internal Logic)28VSSD2-Digital Ground (Internal Logic)28VDD3-5V-Digital Power (5V Power, I/O PAD)30SBCKISub code data ransferring bit clock31JTBOInternal SRAM jitter margin status output32C2POOC2 pointer output33DATXODigital audio data output (48 slot, MSB first)34SADTOOSerial audio data input (48 slot, MSB first)35LRCK0OChannel clock input38LRCKIIChannel clock input39SADTIISerial audio data input (48 slot, MSB first)40VSSD_DACDigital Power for DAC (3V Power)42RCHOUTOReference Voltage output torough DAC43VSSA_DACAnalog Ground for DAC44VREFO <td>15</td> <td>TESTV</td> <td>I</td> <td>Various Data/Clock Input</td>	15	TESTV	I	Various Data/Clock Input
18RESETBISystem Reset at 'L'19MLTILatch signal input from Micom20MDATISerial data input from Micom21MCKISerial data receiving clock input from Micom22ISTATOThe internal status output to Micom23S0S1OSub code sync signal (S0+S1) output24SQCKISub code-Q data transferring bit clock input25SQDTOSub code-Q data serial output26MUTEISystem mute at 'H'27VDDD2-3VDigital Power (3V Power, Internal Logic)28VSSD2-Digital Ground (Internal Logic)28VDD3-5V-Digital Power (5V Power, I/O PAD)30SBCKISub code data transferring bit clock31JITBOInternal SRAM jitter margin status output32C2POOC2 pointer output33DATXODigital audio data output34SADTOOSerial audio data output35LRCKOOChannel clock output36BCKOOBit clock input37BCKIIBit clock input38LRCKIIChannel clock input39SADTIISerial audio data input (48 slot, MSB first)40VSSD_DAC-Digital Ground for DAC41VDDD_DAC-Digital Ground for DAC43VSSA_DAC-Analog Ground for DAC44 <t< td=""><td>16</td><td>LKFS</td><td>0</td><td>The Lock status output of frame sync</td></t<>	16	LKFS	0	The Lock status output of frame sync
19MLTILatch signal input from Micom20MDATISerial data input from Micom21MCKISerial data receiving clock input from Micom22ISTATOThe internal status output to Micom23S0S1OSub code sync signal (S0+S1) output24SQCKISub code-Q data serial output25SQDTOSub code-Q data serial output26MUTEISystem mute at 'H'27VDD2-3VDigital Power (3V Power, Internal Logic)28VSSD2-Digital Ground (Internal Logic)28VDD3-5V-Digital Ground (Internal Logic)30SBCKISub code data transferring bit clock31JITBOInternal SRAM jitter margin status output32C2POOC2 pointer output33DATXODigital audio data output (48 slot, MSB first)34SADTOOSerial audio data output (48 slot, MSB first)35LRCKOOChannel clock output36BCKOOBit clock input37BCKIIBit clock input38LRCKIIChannel clock input39SADTIISerial audio data input (48 slot, MSB first)40VSSD_DAC-Digital Power for DAC (3V Power)41VDDD_DAC-Digital Power for DAC (3V Power)42RCHOUTOReference Voltage output for bypass44VREFO<	17	C4M	0	4.2336MHz clock output
20MDATISerial data input from Micom21MCKISerial data receiving clock input from Micom22ISTATOThe internal status output to Micom23S0S1OSub code sync signal (S0+S1) output24SQCKISub code-Q data serial output25SQDTOSub code-Q data serial output26MUTEISystem mute at 'H'27VDDD2-3VDigital Power (3V Power, Internal Logic)28VSSD2-Digital Ground (Internal Logic)28VSDD3-5V-Digital Power (5V Power, I/O PAD)30SBCKISub code data transferring bit clock31JITBOInternal SRAM jitter margin status output32C2POOC2 pointer output33DATXODigital audio data output (48 slot, MSB first)35LRCKOOBit clock output36BCKIIBit clock input37BCKIIBit clock input38LRCKIIChannel clock input39SADTIISerial audio data input (48 slot, MSB first)40VSSD_DAC-Digital Power for DAC (3V Power)41VDDD_DAC-Digital Power for DAC43VSSA_DAC-Analog Ground for DAC44VREFOReference Voltage output for bypass45VHALFOReference Voltage output for bypass46VDDA_DAC-Analog Power f	18	RESETB	I	System Reset at 'L'
21MCKISerial data receiving clock input from Micom22ISTATOThe internal status output to Micom23SOS1OSub code-sync signal (S0+S1) output24SQCKISub code-Q data transferring bit clock input25SQDTOSub code-Q data serial output26MUTEISystem mute at 'H'27VDDD2-3VDigital Power (3V Power, Internal Logic)28VSSD2-Digital Ground (Internal Logic)28VDD3-5V-Digital Power (5V Power, I/O PAD)30SBCKISub code data transferring bit clock31JITBOInternal SRAM jitter margin status output32C2POOC2 pointer output33DATXODigital audio data output (48 slot, MSB first)35LRCKOOBit clock output36BCKOOBit clock input37BCKIIChannel clock input38LRCKIIChannel clock input39SADTIISerial audio data input (48 slot, MSB first)40VSSD_DAC-Digital Power for DAC41VDD_DAC-Digital Power for DAC43VSSA_DAC-Analog Ground for DAC44VREFOReference Voltage output through DAC45VHALFOReference Voltage output for bypass45VHALFOReference Voltage output for bypass46VDDA_DAC- <td< td=""><td>19</td><td>MLT</td><td>I</td><td>Latch signal input from Micom</td></td<>	19	MLT	I	Latch signal input from Micom
22ISTATOThe internal status output to Micom23S0S1OSub code sync signal (S0+S1) output24SQCKISub code-Q data transferring bit clock input25SQDTOSub code-Q data serial output26MUTEISystem mute at 'H'27VDD2-3V·Digital Power (3V Power, Internal Logic)28VSSD2-Digital Ground (Internal Logic)28VDD3-5V·Digital Power (5V Power, I/O PAD)30SBCKISub code data transferring bit clock31JITBOInternal SRAM jitter margin status output32C2POOC2 pointer output33DATXODigital audio data output (48 slot, MSB first)34SADTOOSerial audio data output35LRCKOOBit clock output36BCKOOBit clock input37BCKIIBit clock input38LRCKIIChannel clock input39SADTIISerial audio data input (48 slot, MSB first)40VSSD_DAC-Digital Power for DAC (3V Power)42RCHOUTOReference Voltage output for bypass45VHALFOReference Voltage output for bypass45VHALFOReference Voltage output for bypass46VDDA_DAC-Analog Power for DAC (3V Power)47LCHOUTOLeft-Channel audio output through DAC	20	MDAT	I	Serial data input from Micom
23SOS1OSub code sync signal (S0+S1) output24SQCKISub code-Q data transferring bit clock input25SQDTOSub code-Q data serial output26MUTEISystem mute at 'H'27VDDD2-3V-Digital Power (3V Power, Internal Logic)28VSSD2-Digital Ground (Internal Logic)28VDD3-5V-Digital Power (5V Power, I/O PAD)30SBCKISub code data transferring bit clock31JITBOInternal SRAM jitter margin status output32C2POOC2 pointer output33DATXODigital audio data output (48 slot, MSB first)35LRCKOOChannel clock output36BCKIIBit clock input37BCKIIBit clock input38LRCKIIChannel clock input39SADTIISerial audio data input (48 slot, MSB first)40VSD_DAC-Digital Ground for DAC41VDD_DAC-Digital Power for DAC (3V Power)42RCHOUTOReference Voltage output for bypass45VHALFOReference Voltage output for bypass46VDA_DAC-Analog Power for DAC (3V Power)47LCHOUTOLeft-Channel audio output through DAC	21	MCK	I	Serial data receiving clock input from Micom
24SQCKISub code-Q data transferring bit clock input25SQDTOSub code-Q data serial output26MUTEISystem mute at 'H'27VDDD2-3V-Digital Power (3V Power, Internal Logic)28VSSD2-Digital Ground (Internal Logic)28VDD3-5V-Digital Ground (Internal Logic)30SBCKISub code data transferring bit clock31JITBOInternal SRAM jitter margin status output32C2POOC2 pointer output33DATXODigital audio data output (48 slot, MSB first)35LRCKOOChannel clock output36BCKIIBit clock input37BCKIIBit clock input38LRCKIIChannel clock input39SADTIISerial audio data input (48 slot, MSB first)40VSSD_DAC-Digital Ground for DAC41VDD_DAC-Digital Power for DAC (3V Power)42RCHOUTOReference Voltage output for bypass45VHALFOReference Voltage output for bypass46VDDA_DAC-Analog Power for DAC (3V Power)47LCHOUTOLeft-Channel audio output through DAC	22	ISTAT	0	The internal status output to Micom
25SQDTOSub code-Q data serial output26MUTEISystem mute at 'H'27VDDD2-3VDigital Power (3V Power, Internal Logic)28VSSD2-Digital Ground (Internal Logic)28VDD3-5V-Digital Power (5V Power, I/O PAD)30SBCKISub code data transferring bit clock31JITBOInternal SRAM jitter margin status output32C2POOC2 pointer output33DATXODigital audio data output34SADTOOSerial audio data output (48 slot, MSB first)35LRCKOOChannel clock output36BCKOOBit clock input37BCKIIBit clock input38LRCKIIChannel clock input39SADTIISerial audio data input (48 slot, MSB first)40VSSD_DAC-Digital Power for DAC41VDD_DAC-Digital Power for DAC (3V Power)42RCHOUTOReference Voltage output for bypass45VHALFOReference Voltage output for bypass46VDA_DAC-Analog Power for DAC (3V Power)47LCHOUTOLeft-Channel audio output through DAC	23	S0S1	0	Sub code sync signal (S0+S1) output
26MUTEISystem mute at 'H'27VDDD2-3V-Digital Power (3V Power, Internal Logic)28VSSD2-Digital Ground (Internal Logic)28VDD3-5V-Digital Power (5V Power, I/O PAD)30SBCKISub code data transferring bit clock31JITBOInternal SRAM jitter margin status output32C2POOC2 pointer output33DATXODigital audio data output34SADTOOSerial audio data output (48 slot, MSB first)35LRCKOOChannel clock output36BCKOOBit clock input37BCKIIBit clock input38LRCKIIChannel clock input39SADTIISerial audio data input (48 slot, MSB first)40VSSD_DAC-Digital Ground for DAC41VDD_DAC-Digital Power for DAC (3V Power)42RCHOUTORight-Channel audio output through DAC44VREFOReference Voltage output for bypass45VHALFOReference Voltage output for bypass46VDDA_DAC-Analog Power for DAC (3V Power)47LCHOUTOLeft-Channel audio output through DAC	24	SQCK	I	Sub code-Q data transferring bit clock input
27VDDD2-3V-Digital Power (3V Power, Internal Logic)28VSSD2-Digital Ground (Internal Logic)28VDD3-5V-Digital Power (5V Power, I/O PAD)30SBCKISub code data transferring bit clock31JITBOInternal SRAM jitter margin status output32C2POOC2 pointer output33DATXODigital audio data output (48 slot, MSB first)34SADTOOSerial audio data output (48 slot, MSB first)35LRCKOOChannel clock output36BCKOOBit clock input38LRCKIIBit clock input39SADTIISerial audio data input (48 slot, MSB first)40VSSD_DAC-Digital Ground for DAC41VDDD_DAC-Digital Power for DAC (3V Power)42RCHOUTOReference Voltage output for bypass45VHALFOReference Voltage output for bypass46VDDA_DAC-Analog Power for DAC (3V Power)47LCHOUTOLeft-Channel audio output through DAC	25	SQDT	0	Sub code-Q data serial output
21VSD2-SVDigital Fower (SV Fower, Internal Logic)28VSSD2-Digital Ground (Internal Logic)28VDD3-5V-Digital Power (SV Power, I/O PAD)30SBCKISub code data transferring bit clock31JITBOInternal SRAM jitter margin status output32C2POOC2 pointer output33DATXODigital audio data output34SADTOOSerial audio data output (48 slot, MSB first)35LRCKOOChannel clock output36BCKOOBit clock output37BCKIIBit clock input39SADTIISerial audio data input (48 slot, MSB first)40VSSD_DAC-Digital Ground for DAC41VDDD_DAC-Digital Power for DAC (3V Power)42RCHOUTOReference Voltage output for bypass45VHALFOReference Voltage output for bypass46VDDA_DAC-Analog Power for DAC (3V Power)47LCHOUTOLeft-Channel audio output through DAC	26	MUTE	I	System mute at 'H'
28VDDD3-5V-Digital Power (5V Power, I/O PAD)30SBCKISub code data transferring bit clock31JITBOInternal SRAM jitter margin status output32C2POOC2 pointer output33DATXODigital audio data output34SADTOOSerial audio data output (48 slot, MSB first)35LRCKOOChannel clock output36BCKOOBit clock input37BCKIIBit clock input38LRCKIIChannel clock input39SADTIISerial audio data input (48 slot, MSB first)40VSSD_DAC-Digital Ground for DAC41VDDD_DAC-Digital Power for DAC (3V Power)42RCHOUTOReference Voltage output for bypass44VREFOReference Voltage output for bypass45VHALFOReference Voltage output for bypass46VDDA_DAC-Analog Power for DAC (3V Power)47LCHOUTOLeft-Channel audio output through DAC	27	VDDD2-3V	-	Digital Power (3V Power, Internal Logic)
30SBCKISub code data transferring bit clock31JITBOInternal SRAM jitter margin status output32C2POOC2 pointer output33DATXODigital audio data output34SADTOOSerial audio data output (48 slot, MSB first)35LRCKOOChannel clock output36BCKOOBit clock input37BCKIIBit clock input38LRCKIIChannel clock input39SADTIISerial audio data input (48 slot, MSB first)40VSSD_DAC-Digital Ground for DAC41VDDD_DAC-Digital Power for DAC (3V Power)42RCHOUTORight-Channel audio output through DAC43VSSA_DAC-Analog Ground for DAC44VREFOReference Voltage output for bypass46VDDA_DAC-Analog Power for DAC (3V Power)47LCHOUTOLeft-Channel audio output through DAC	28	VSSD2	-	Digital Ground (Internal Logic)
31JITBOInternal SRAM jitter margin status output32C2POOC2 pointer output33DATXODigital audio data output34SADTOOSerial audio data output (48 slot, MSB first)35LRCKOOChannel clock output36BCKOOBit clock output37BCKIIBit clock input38LRCKIIChannel clock input39SADTIISerial audio data input (48 slot, MSB first)40VSSD_DAC-Digital Ground for DAC41VDDD_DAC-Digital Power for DAC (3V Power)42RCHOUTORight-Channel audio output through DAC43VSSA_DAC-Analog Ground for DAC44VREFOReference Voltage output for bypass45VHALFOReference Voltage output for bypass46VDDA_DAC-Analog Power for DAC (3V Power)47LCHOUTOLeft-Channel audio output through DAC	28	VDDD3-5V	-	Digital Power (5V Power, I/O PAD)
32C2POOC2 pointer output33DATXODigital audio data output34SADTOOSerial audio data output (48 slot, MSB first)35LRCKOOChannel clock output36BCKOOBit clock output37BCKIIBit clock input38LRCKIIChannel clock input39SADTIISerial audio data input (48 slot, MSB first)40VSSD_DAC-Digital Ground for DAC41VDDD_DAC-Digital Power for DAC (3V Power)42RCHOUTORight-Channel audio output through DAC43VREFOReference Voltage output for bypass45VHALFOReference Voltage output for bypass46VDDA_DAC-Analog Power for DAC (3V Power)47LCHOUTOLeft-Channel audio output through DAC	30	SBCK	I	Sub code data transferring bit clock
33DATXODigital audio data output34SADTOOSerial audio data output (48 slot, MSB first)35LRCKOOChannel clock output36BCKOOBit clock output37BCKIIBit clock input38LRCKIIChannel clock input39SADTIISerial audio data input (48 slot, MSB first)40VSSD_DAC-Digital Ground for DAC41VDDD_DAC-Digital Power for DAC (3V Power)42RCHOUTORight-Channel audio output through DAC43VSSA_DAC-Analog Ground for DAC44VREFOReference Voltage output for bypass46VDDA_DAC-Analog Power for DAC (3V Power)47LCHOUTOLeft-Channel audio output through DAC	31	JITB	0	Internal SRAM jitter margin status output
34SADTOOSerial audio data output (48 slot, MSB first)35LRCKOOChannel clock output36BCKOOBit clock output37BCKIIBit clock input38LRCKIIChannel clock input39SADTIISerial audio data input (48 slot, MSB first)40VSSD_DAC-Digital Ground for DAC41VDDD_DAC-Digital Power for DAC (3V Power)42RCHOUTORight-Channel audio output through DAC43VSSA_DAC-Analog Ground for DAC44VREFOReference Voltage output for bypass45VHALFOReference Voltage output for bypass46VDDA_DAC-Analog Power for DAC (3V Power)47LCHOUTOLeft-Channel audio output through DAC	32	C2PO	0	C2 pointer output
35LRCKOOChannel clock output36BCKOOBit clock output37BCKIIBit clock input38LRCKIIChannel clock input39SADTIISerial audio data input (48 slot, MSB first)40VSSD_DAC-Digital Ground for DAC41VDDD_DAC-Digital Power for DAC (3V Power)42RCHOUTORight-Channel audio output through DAC43VSSA_DAC-Analog Ground for DAC44VREFOReference Voltage output for bypass45VHALFOReference Voltage output for bypass46VDDA_DAC-Analog Power for DAC (3V Power)47LCHOUTOLeft-Channel audio output through DAC	33	DATX	0	Digital audio data output
36BCKOOBit clock output37BCKIIBit clock input38LRCKIIChannel clock input39SADTIISerial audio data input (48 slot, MSB first)40VSSD_DAC-Digital Ground for DAC41VDDD_DAC-Digital Power for DAC (3V Power)42RCHOUTORight-Channel audio output through DAC43VSSA_DAC-Analog Ground for DAC44VREFOReference Voltage output for bypass45VHALFOReference Voltage output for bypass46VDDA_DAC-Analog Power for DAC (3V Power)47LCHOUTOLeft-Channel audio output through DAC	34	SADTO	0	Serial audio data output (48 slot, MSB first)
37BCKIIBit clock input38LRCKIIChannel clock input39SADTIISerial audio data input (48 slot, MSB first)40VSSD_DAC-Digital Ground for DAC41VDDD_DAC-Digital Power for DAC (3V Power)42RCHOUTORight-Channel audio output through DAC43VSSA_DAC-Analog Ground for DAC44VREFOReference Voltage output for bypass45VHALFOReference Voltage output for bypass46VDDA_DAC-Analog Power for DAC (3V Power)47LCHOUTOLeft-Channel audio output through DAC	35	LRCKO	0	Channel clock output
38LRCKIIChannel clock input39SADTIISerial audio data input (48 slot, MSB first)40VSSD_DAC-Digital Ground for DAC41VDDD_DAC-Digital Power for DAC (3V Power)42RCHOUTORight-Channel audio output through DAC43VSSA_DAC-Analog Ground for DAC44VREFOReference Voltage output for bypass45VHALFOReference Voltage output for bypass46VDDA_DAC-Analog Power for DAC (3V Power)47LCHOUTOLeft-Channel audio output through DAC	36	BCKO	0	Bit clock output
39SADTIISerial audio data input (48 slot, MSB first)40VSSD_DAC-Digital Ground for DAC41VDDD_DAC-Digital Power for DAC (3V Power)42RCHOUTORight-Channel audio output through DAC43VSSA_DAC-Analog Ground for DAC44VREFOReference Voltage output for bypass45VHALFOReference Voltage output for bypass46VDDA_DAC-Analog Power for DAC (3V Power)47LCHOUTOLeft-Channel audio output through DAC	37	BCKI	I	Bit clock input
39SADTIISerial audio data input (48 slot, MSB first)40VSSD_DAC-Digital Ground for DAC41VDDD_DAC-Digital Power for DAC (3V Power)42RCHOUTORight-Channel audio output through DAC43VSSA_DAC-Analog Ground for DAC44VREFOReference Voltage output for bypass45VHALFOReference Voltage output for bypass46VDDA_DAC-Analog Power for DAC (3V Power)47LCHOUTOLeft-Channel audio output through DAC	38	LRCKI	I	Channel clock input
40VSSD_DAC-Digital Ground for DAC41VDDD_DAC-Digital Power for DAC (3V Power)42RCHOUTORight-Channel audio output through DAC43VSSA_DAC-Analog Ground for DAC44VREFOReference Voltage output for bypass45VHALFOReference Voltage output for bypass46VDDA_DAC-Analog Power for DAC (3V Power)47LCHOUTOLeft-Channel audio output through DAC			I	· · · · · · · · · · · · · · · · · · ·
41VDDD_DAC-Digital Power for DAC (3V Power)42RCHOUTORight-Channel audio output through DAC43VSSA_DAC-Analog Ground for DAC44VREFOReference Voltage output for bypass45VHALFOReference Voltage output for bypass46VDDA_DAC-Analog Power for DAC (3V Power)47LCHOUTOLeft-Channel audio output through DAC			-	
42RCHOUTORight-Channel audio output through DAC43VSSA_DAC-Analog Ground for DAC44VREFOReference Voltage output for bypass45VHALFOReference Voltage output for bypass46VDDA_DAC-Analog Power for DAC (3V Power)47LCHOUTOLeft-Channel audio output through DAC			-	
43       VSSA_DAC       -       Analog Ground for DAC         44       VREF       O       Reference Voltage output for bypass         45       VHALF       O       Reference Voltage output for bypass         46       VDDA_DAC       -       Analog Power for DAC (3V Power)         47       LCHOUT       O       Left-Channel audio output through DAC	42	RCHOUT	0	
44VREFOReference Voltage output for bypass45VHALFOReference Voltage output for bypass46VDDA_DAC-Analog Power for DAC (3V Power)47LCHOUTOLeft-Channel audio output through DAC	43			
45VHALFOReference Voltage output for bypass46VDDA_DAC-Analog Power for DAC (3V Power)47LCHOUTOLeft-Channel audio output through DAC			0	
46     VDDA_DAC     -     Analog Power for DAC (3V Power)       47     LCHOUT     O     Left-Channel audio output through DAC				
47 LCHOUT O Left-Channel audio output through DAC				
			-	

#### ■ BA3837 (IC301) : Mic. mixer

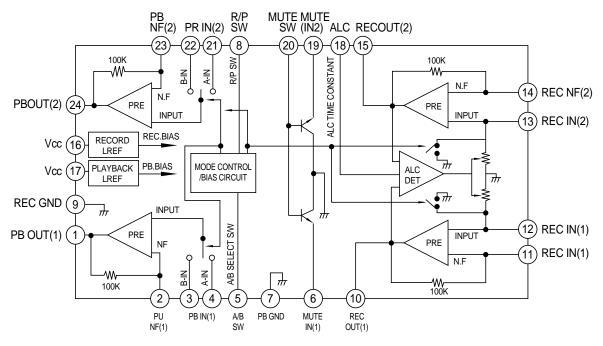
#### 1.Block diagram



#### 2.Pin function

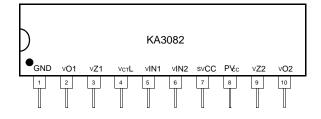
Pin No.	Symbol	I/O	Function
1	VCC	-	Power supply
2	MIC IN	I	Microphone mixing input
3	LOUT	0	Channel L output
4	FK	-	Non connect
5	TK	-	Non connect
6	LIN	I	Channel L input
7	BIAS		Signal bias
8	GND	-	Connect to GND
9	RIN	Ι	Channel R input
10	LPF1	0	Connects to LPF time constant element
11	LPF2	0	Connects to LPF time constant element
12	LPF3	0	LPF output
13	ROUT	0	Channel R output
14	CONTA		Mode select input A
15	CONTB		Mode select input B
16	CONTC	I	Mode select input C

# ■ KA22291 (JIC1) : Cassette amp.



# ■ KA3082 (SIC4) : Bidirectional DC motor driver

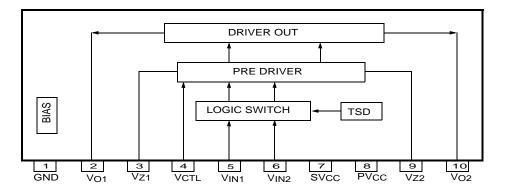
1.Pin layout



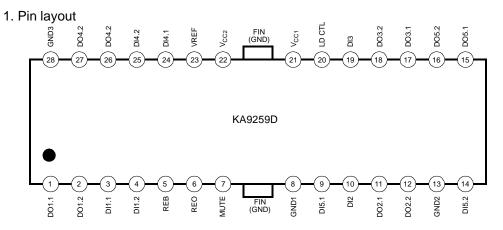
#### 2.Pin function

Pin No.	Symbol	Туре	Function
1	GND	-	Ground
2	VO1	0	Output 1
3	Vz1	-	Phase compensation
4	VCTL	I	Motor speed control
5	VIN1	I	Input 1
6	VIN2	I	Input 2
7	SVCC	-	Supply voltage (Signal)
8	PVcc	-	Supply voltage (Power)
9	V <sub>Z2</sub>	-	Phase compensation
10	V <sub>O2</sub>	0	Ooutput 2

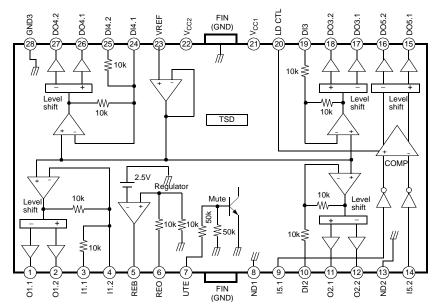
#### 3.Block Diagram



# KA9259D (SIC3) : 5-ch Motor driver



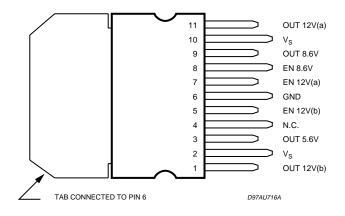
## 2. Block diagram



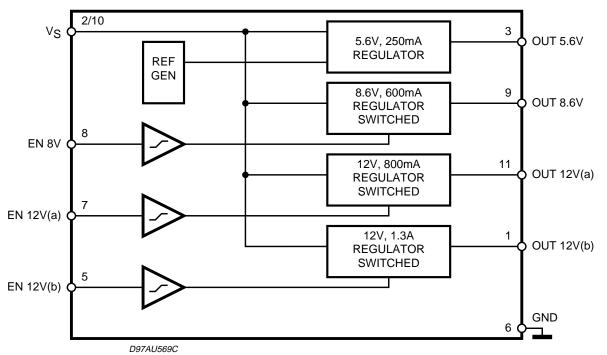
Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	DO1.1	0	Focus output 1 (-)	15	DO5.1	0	Loading output 1(+)
2	DO1.2	0	Focus output 2 (+)	16	DO5.2	0	Loading output 2(-)
3	DI1.1	Ι	Focus input 1	17	DO3.1	0	Sled output (-)
4	DI1.2	Ι	Focus input 2 (Adjustable)	18	DO3.2	0	Sled output (+)
5	REB	0	Regulator base	19	DI3	I	Sled input
6	REO	0	Regulator output, 5V	20	LD CTL	Ι	Loading motor speed control
7	MUTE	Ι	Mute	21	V <sub>CC1</sub>	-	Supply voltage 1
8	GND1	-	Ground 1	22	V <sub>CC2</sub>	-	Supply voltage 2
9	DI5.1	Ι	Loading input 1	23	VREF	Ι	2.5V bias
10	DI2	Ι	Spindle input 2	24	DI4.1	Ι	Tracking input 1 (Adjustable)
11	DO2.1	0	Spindle output (+)	25	DI4.2	Ι	Tracking input 2
12	DO2.2	0	Spindle output (-)	26	DO4.1	0	Tracking output 1 (+)
13	GND2	-	Ground 2	27	DO4.2	0	Tracking output 2 (-)
14	DI5.2	Ι	Loading input 2	28	GND3	l	Ground 3

# ■ L4959 (RIC1) : Voltage regulator

1.Pin layout



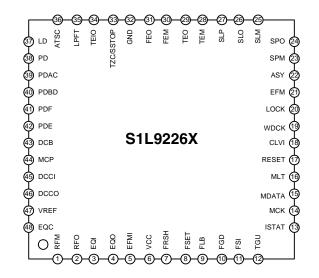
## 2.Block diagram



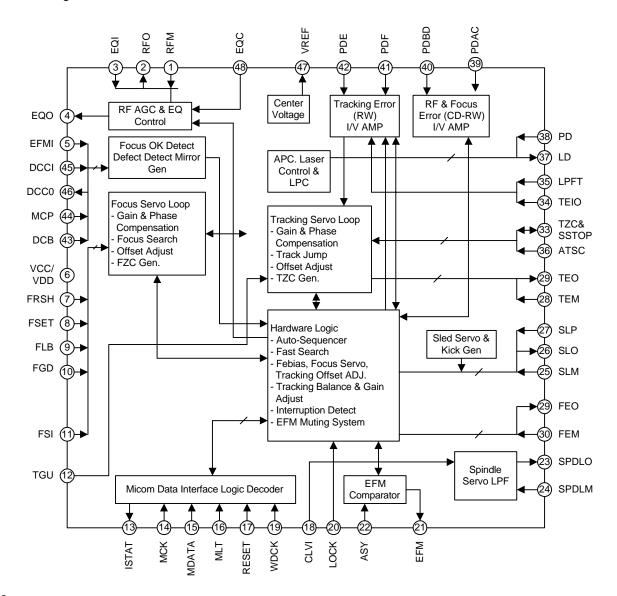
Pin No.	Symbol	Function
1	OUT 12V (b)	12V/1.3A SWITCHED OUTPUT VOLTAGE
2	Vs	Supply Voltage
3	OUT 5.6V	5.6V/250mA OUTPUT VOLTAGE
4	N.C.	not connected
5	EN 12V (b)	Enable 12V/1.3A SWITCHED OUTPUT VOLTAGE
6	GND	Ground
7	EN 12V (a)	Enable 12V/0.8A SWITCHED OUTPUT VOLTAGE
8	EN 8.6V	Enable 8.6V/0.6A SWITCHED OUTPUT VOLTAGE
9	OUT 8.6	8.6V/0.6A SWITCHED OUTPUT VOLTAGE
10	Vs	Supply Voltage
11	OUT 12V (a)	12V/0.8A SWITCHED OUTPUT VOLTAGE

# KB9226 (IC101) : RF amp. & Servo signal processor

1. Pin layout

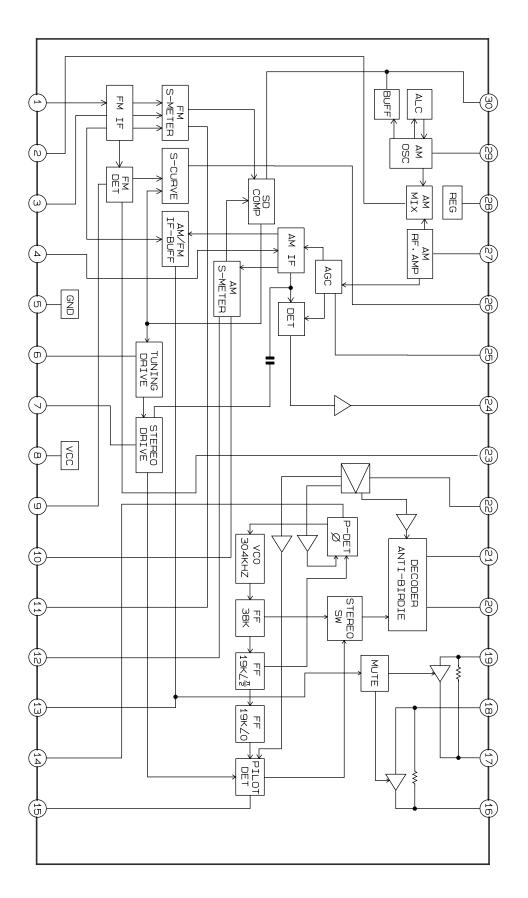


2. Block diagram



3. Pin fun	ction		KB9226			
Pin No.	Symbol	Туре	Function			
1	RFM	I	RF summing amp. inverting input			
2	RFO	0	RF summing amp. output			
3	EQI	I	RFO DC eliminating input(use by MIRROR, FOK ,AGC & EQ terminal)			
4	EQO	0	RF equalizer output			
5	EFMI	I	EFM slice input. (input impedance 47K)			
6	VCC	Р	Main power supply			
7	FRSH	I	Capacitor connection to focus search			
8	FSET	I	Filter bias for focus, tracking, spindle			
9	FLB	I	Capacitor connection to make focus loop rising band			
10	FGD	I	Terminal to change the hign frequency gain of focus loop			
11	FSI	I	Focus servo input			
12	TGU	I	Connect the component to change the high frequency of tracking Loop			
13	ISTAT	0	Internal status output			
14	MCK	I	Micom clock			
15	MDATA	I	Data input			
16	MLT	I	Data latch input			
17	RESET	I	Reset input			
18	CLVI	I	Input the spindle control output from DSP			
19	WDCK	I	88.2KHz input terminal from DSP			
20	LOCK	I	Sled run away inhibit pin (L: sled off & tracking gain up)			
21	EFM	0	EFM output for RFO slice(to DSP)			
22	ASY	I	Auto asymmetry control input			
23	SPM	I	Spindle amp. inverting input			
24	SPO	0	Spindle amp. output			
25	SLM	I	Sled servo inverting input			
26	SLO	0	Sled servo output			
27	SLP	I	Sled servo non inverting input			
28	TEM	I	Tracking servo amp.inverting input			
29	TEO	0	Tracking servo amp. output			
30	FEM	I	Focus servo amp. inverting input			
31	FEO	0	Focus servo amp. output pin			
32	GND	Р	Main ground			
33	TZC/ SSTOP	I	Tracking zero crossing input & Check the position of pick-up whether inside or not			
34	TEIO	В	Tracking error output & Tracking servo input			
35	LPFT	I	Tracking error integration input (to automatic control)			
36	ATSC	I	Anti-shock input			
37	LD	0	APC amp. output			
38	PD	I	APC amp. input			
39	PDAC	I	Photo diode A & C RF I/V amp. inverting input			
40	PDBD		Photo diode B & D RF I/V amp. inverting input			
41	PDF		Photo diode F & tracking(F) I/V amp. inverting input			
42	PDE	I	Photo diode E & tracking(E) I/V amp. inverting input			
43	DCB	I	Capacitor connection to limit the defect detection			
44	MCP	I	Capacitor connection to mirror hold			
45	DCCI	0	Output pin to connect the component for defect detect			
46	DCCO	I	Input pin to connect the component for defect detect			
47	VREF	0	(VCC+GND)/2 Voltage reference output			
48	EQC	I	AGC_equalize level control terminal & capacitor terminal to input in to VCA			

# LA1837 (IC01) : FM IF/DET AM RF/IF/DET

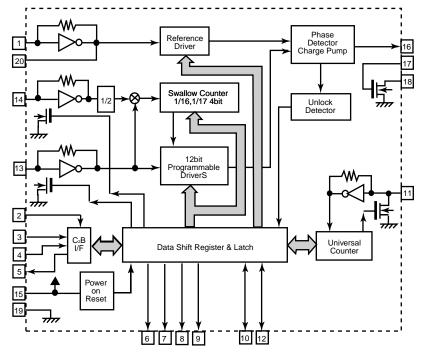


# ■ LC72131M (IC02) : PLL frequency synthesizer

1. Pin layout

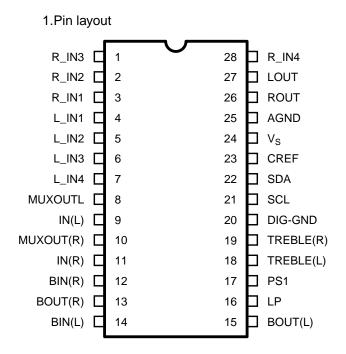
XIN	1	20	XOUT
CE	2	19	Vss
DI	3	18	AOUT
CL	4	17	AIN
DO	5	16	PD
BO1	6	15	VDD
BO2	7	14	FMIN
BO3	8	13	AMIN
BO4	9	12	IO2
B04	9	12	IO2
101	10	11	IFIN

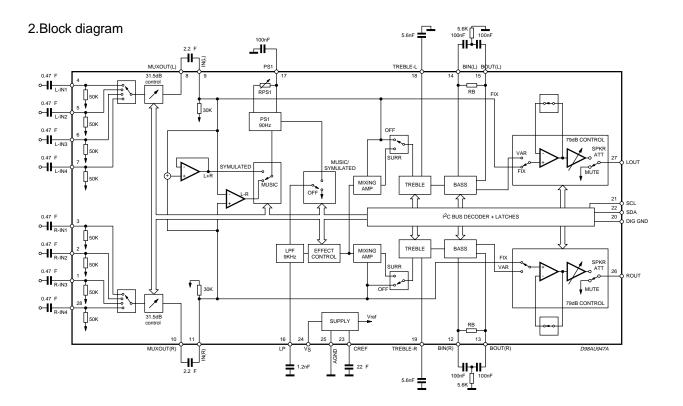
2. Block diagram



Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	XIN	I	X'tal oscillator connect (4.5MHz/7.2MHz)	11	IFIN	I	IF counter signal input
2	CE	-	Chip enable	12	IO2	I/O	I/O port
3	DI	I	Input data	13	AMIN	I	AM Local oscillator signal input
4	CL	I	Clook	14	FMIN	I	FM Local oscillator signal input
5	DO	0	Output data	15	VDD	Ι	Power suplly(VDD=4.5-5.5V)
6	BO1	0	Output port	16	PD	0	Charge pump output
7	BO2	0	Output port	17	AIN	I	Low-pass filter
8	BO3	0	Output port	18	AOUT	0	Amplifier Tr
9	BO4	0	Output port	19	GND	-	Connected to GND
10	ĪO1	I/O	I/O port	20	XOUT	I	X'tal oscillator connect (4.5MHz/7.2MHz)

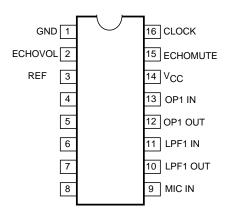
# ■ TDA7442D (FIC1) : Audio processor





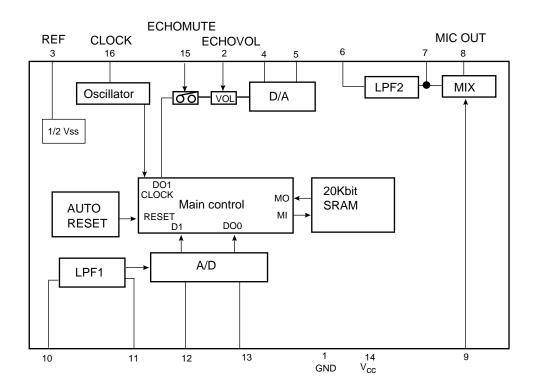
# ■ M65855FP (EIC1) : Sound processor

## 1. Pin layout



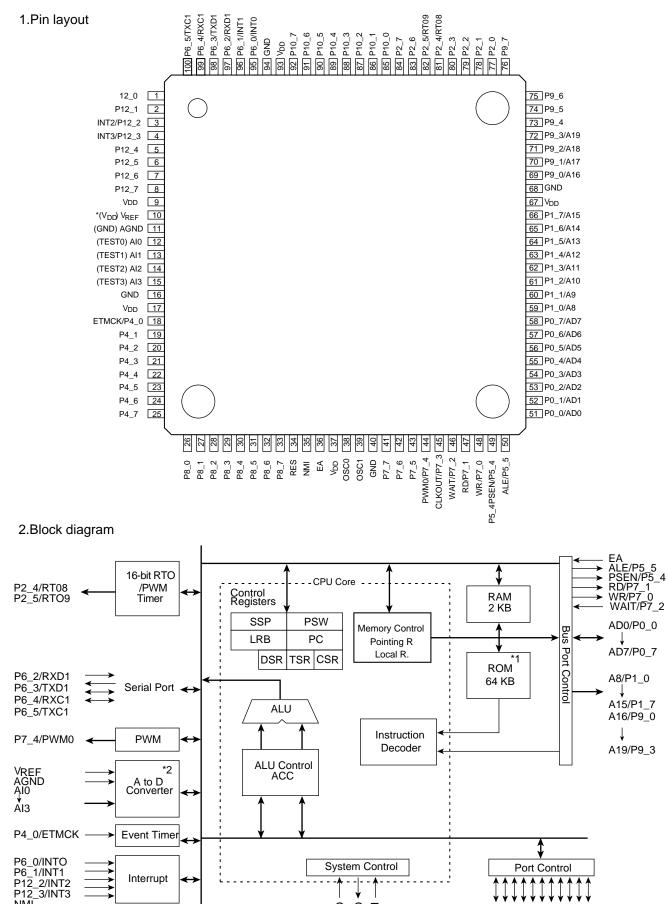
Pin No.	Symbol	Function	
1	GND		
2	ECHOVOL	Echo level control with external DC voltage	
3	REF	To connect 1/2 Vcc output and filter capacitor	
4	OP2 IN	Uses external C to from an D/A conversion	
5	OP2 OUT	integrator	
6	LPF2 IN	Uses external CR to from a low pass filter at the	
7	LPF2 OUT	input side	
8	MIC OUT	Mixing output echo output and microphone	
9	MIC IN	Microphone input	
10	LPF1 OUT	Uses external CR to from a low pass filter at the	
11	LPF1 IN	input side	
12	OP1 OUT	Uses external C to from an D/A conversion	
13	OP1 IN	integrator	
14	V <sub>CC</sub>	Applies a voltage of 3.5V to 5.5V(Rated5V)	
15	ECHOMUTE	Echo mute control and clock stop control with external DC voltage	
16	CLOCK	Controls a built -in clock generation circuit with external R	

3. Block diagram



## MX-K55V

# MSM66587 (MIC1) : Microprocessor



OSC0 - OSC1 RES

987679999999 042456

NM

P7\_3/CLKOUT ~

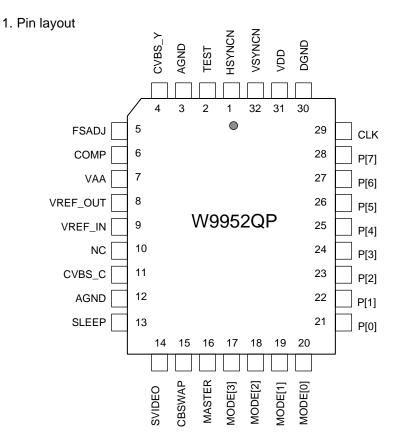
Peripheral

## 3.Pin function

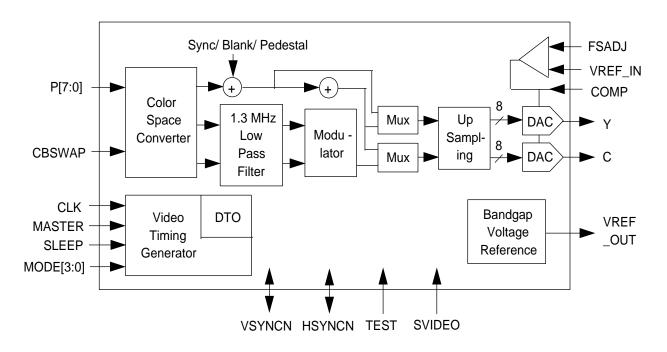
MSM66587

			MSM66587
Pin No.	Symbol	I/O	Function
1~2	P12_0~P12~2	I/O	Input or output can be specified for each bit with the port 12 Mode Register
3	INT2/P12_2	I/O	Input or output can be specified for each bit with the port 12 Mode Register
4	INT3/P12_3	I/O	Input or output can be specified for each bit with the port 12 Mode Register
5~8	P12_4~P12_7	I/O	Input or output can be specified for each bit with the port 12 Mode Register
9	VDD	I	Power supply +5V
10	(VDD) VREF	I	This is the reference voltage pin for the A/D converter (VDD for MSM66585).
11	(GND) AGND	I	This is the ground input pin for the A/D converter (GND for MSM66585).
12~15	(TEST0) AI0~AI3	Ι	These are analog input pins for the A/D converter (test pins for MSM66585).
16	GND	Ι	Connect to GND
17	VDD	Ι	Power supply +5V
18	EIMOK/P4_0	I	Input or output can be specified for each bit with the port 4 Mode Register
19~25	P4_1~P4_7	Ι	Input or output can be specified for each bit with the port 4 Mode Register
26~33	P8_0~P8_7	I	Input or output can be specified for each bit with the port 8 Mode Register
34	RES	I	This is an active-low reset input pin.
35	NMI	Ι	This input pin requests a non-maskable interrupt.
36	EA	Ι	When this pin is low, all program addresses will access external program memory.
37	VDD	I	Power supply +5V
38	OSO0	I	This pins connect to a crystal oscillator.
39	OSC1	0	This pins connect to a crystal oscillator.
40	GND	Ι	Connect to GND
41~43	P7_5~P7_7	I/O	Input or output can be specified for each bit with the port 7 Mode Register
44	PWN0/P7_4	I/O	Input or output can be specified for each bit with the port 7 Mode Register
45	CLKOUT/P7_3	I/O	Input or output can be specified for each bit with the port 7 Mode Register
46	WAIT/P7_2	I/O	Input or output can be specified for each bit with the port 7 Mode Register
47	RD/P7_1	I/O	Input or output can be specified for each bit with the port 7 Mode Register
48	WR/P7_0	I/O	Input or output can be specified for each bit with the port 7 Mode Register
49	P5_4PSEN/P5_4	I/O	Input or output can be specified for each bit with the port 5 Mode Register
50	ALE/P5_5	I/O	Input or output can be specified for each bit with the port 5 Mode Register
51~58	P0_0~7/AD0~AD7	I/O	Input or output can be specified for each bit with the port 0 Mode Register
59~66	P1_0~7/A8~A15	I/O	Input or output can be specified for each bit with the port 1 Mode Register
67	VDD	Ι	Power supply +5V
68	GND	I	Connect to GND
69~72	P9_0~3/A16~A19	I/O	Input or output can be specified for each bit with the port 9 Mode Register
73~76	P9_4~P9_7	I/O	Input or output can be specified for each bit with the port 9 Mode Register
77~80	P2_0~P2_3	I/O	Input or output can be specified for each bit with the port 2 Mode Register
81	P2_4/RT08	I/O	Input or output can be specified for each bit with the port 2 Mode Register
82	P2_5/RT09	I/O	Input or output can be specified for each bit with the port 2 Mode Register
83~84	P2_6~P2_7	I/O	Input or output can be specified for each bit with the port 2 Mode Register
85~92	P10_1~P10_7	I/O	Input or output can be specified for each bit with the port 10 Mode Register
93	VDD	I	Power supply +5V
94	GND	I	Connect to GND
95~96	P6_0~1/INT0~1	I/O	Input or output can be specified for each bit with the port 6 Mode Register
97	P6_2/RXD1	I/O	Input or output can be specified for each bit with the port 6 Mode Register
98	P6_3/TXD1	I/O	Input or output can be specified for each bit with the port 6 Mode Register
99	P6_4/TXD1	I/O	Input or output can be specified for each bit with the port 6 Mode Register
100	P6_5/RXC1	I/O	Input or output can be specified for each bit with the port 6 Mode Register

# ■ W9952QP (MIC3) : Video decoder



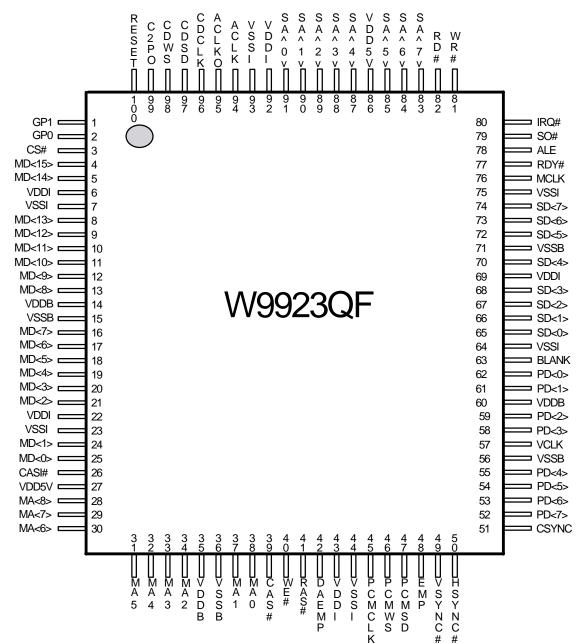
#### 2. Block diagram.



Pin No.	Туре	I/O	Function
21-28	P[7:0]	Ι	YCrCb pixel inputs. They are latched on the falling edge of CLK. YCrCb input data conform to CCIR 601.
29	CLK	I	2x Pixel clock input for 8-bit YCrCb data.
32	VSYNCN	I/O	Vertical sync input/output. VSYNCN is latched/output following the rising edge of CLK.
1	HSYNCN	I/O	Horizontal sync input/output. HSYNCN is latched/output following the rising edge of CLK.
16	MASTER	I	Master/slave mode select. A logical high for master mode operation. A logical 0 for slave mode operation
15	CBSWAP	I	Cr and Cb pixel sequence set up pin. A logic high swap the Cr and Cb sequence.
14	SVIDEO	I	SVIDEO select input pin. A logic high selects Y/C output. A logic low selects composite video output.
13	SLEEP	I	Power save mode. A logic high on this pin puts the chip into power-down mode.
17-20	Mode[3:0]	I	Mode configuration pin.
2	TEST	I	Test pin. These pins must be connected to DGND.
9	VREF_IN		Voltage reference input. An external voltage reference must supply typical 1.235V to this pin. A 0.1uF ceramic capacitor must be used to decouple this input to GND. The decoupling capacitor must be as close as possible to minimize the length of the load. This pin may be connected directly to VREF_OUT.
8	VREF_OUT	0	Voltage reference output. It generates typical 1.2V voltage reference and may be used to drive VREF_IN pin directly.
5	FSADJ		Full-Scale adjust control pin. The Full-Scale current of D/A converters can be adjusted by connecting a resistor (RSET) between this pin and ground. The relationship is
6	COMP		Compensation pin. A 0.1uF ceramic capacitor must be used to bypass this pin to VAA. The lead length must be kept as short as possible to avoid noise.
4	CVBS_Y	0	Composite/Luminance output. This is a high-impedance current source output. The output format can be selected by the PAL pin. The pin can drive a 37.5 W load. If unused, this pin must be connected directly to GND.
11	CVBS_C	0	Composite/Chroma output. This is a high impedance current source Output. The output format can be selected by the PAL pin. The pin can drive a 37.5 W load. If unused, this pin must be connected directly to GND.
10	NC		No connection
31	VDD		Digital power pin
30	DGND		Digital ground pin
7	VAA		Analog power pin
3,12	AGND		Analog ground pin

# ■ W9923QF (MIC4) : MPEG decoder

1. Pin layout



## 2 Pin function

(1/2)

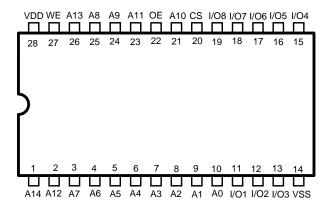
Pin No.	Symbol	type	Function
1~2	GP0~1	I/O	Programmable input/output 1
3	CS#		Chip select input, active LOW; optional
4~5	MD<14~15>	I/O	DRAM data bus
6,14,22,35	VDD		3.3V power supply
7,15,23,36,44	VSS		0V ground
8~13	MD<8~13>	I/O	DRAM data bus
16~21	MD<2~7>	I/O	DRAM data bus
24~25	MD<0~1>	I/O	DRAM data bus
26	CASIN#		Column address strobe input to lach data from DRAM, rising edge active

(2/2)

			(L/L)			
Pin No.	Symbol	type	Function			
27	VDD5V		5V power supply			
28~34	MA<2~8>	0	DRAM address bus			
37~38	MA<0~1>	0	DRAM address bus			
39	CS#	0	Column address strobe output, falling edge active			
40	WE#	0	Write enableoutput, active LOW to indicate write operation to DRAM			
41	RAS#	0	Row address strobe output, falling edge active			
42	DAEMP		DA emphasis input, active HIGH			
43,60,69,92	VDD		3.3V power supply			
45	PCMCLK	0	Audio PCM clock output			
46	PCMWS	0	PCM channel word selector, active HIGH, programmable			
47	PCMSD	0	Audio PCM serial data output			
48	EMP	0	Audio emphasis flag, active HIGH			
49	VSYNC#	I/O	Vertical synch, active LOW, input/output programmable, default in INPUT state			
50	HSYNC#	I/O	Horizontal sync, active LOW, input/output programmable, default in INPUT state			
51	CSYNC	0	Composite sync signal, active LOW			
52~55	PD<4~7>	0	Pixel Data bus			
57	VCLK	I/O	Video clock, usually 27MHz for TV scan, twice the luminance rate, input/output programmable, default in INPUT state			
58~59	PD<2~3>	0	Pixel Data bus			
61~62	PD<0~1>	0	Pixel Data bus			
63	BLANK#	0	Composite blank, active LOW HSYNC# are in input state			
64,71,75,93	VSS		0V ground			
65~68,70	SD<0~3,4>	I/O	System data bus			
72~73	SD<5~7>	I/O	System data bus			
76	MCLK	1	Main clock input, typically 40.5MHz			
77	BUSY#	0	Bus BUSY, LOW indicates bus busy, open			
78	ALE		Active HIGH, address latch enable for 8051			
79	SO	0	Address select output, valid from IOAR+10h to IOAR+2fh (total 32 byteaddresses), active LOW			
80	IRQ#	0	Interrupt request output, active when an interrupt event is triggered active LOW			
81	WR#	I	write enable, active LOW			
82	RD#	I	Read enable, active LOW			
83~85	SA<5~7>		System address bus			
86	VDD5V		3.3V power supply			
87~91	SA<0~4>		System address bus			
94	ACLK	I	Optional secondary clock for audio sampling rate, PCM clock			
95	ACLKO	0	ACLK output, ACLK and ACLKO are used for crystal input pins			
96	CDCLK	I	CD bit clock input			
		-				
97	CDSD	I	CD senai data input			
97 98			CD serial data input CD data word selector			
	CDSD CDWS C2PO		CD serial data input CD data word selector CD data byte erasure flag			

# ■ W24257 (MIC2) : SRAM

### 1. Pin layout



#### 2. Pin function

Pin No.	Symbol	Туре	Function
1	A14	I	Address input
2	A12	I	Address input
3	A7	I	Address input
4	A6	I	Address input
5	A5	I	Address input
6	A4	I	Address input
7	A3	I	Address input
8	A2	I	Address input
9	A1	I	Address input
10	A0	I	Data Input/Output
11	I/O1	I/O	Data Input/Output
12	I/O2	I/O	Data Input/Output
13	I/O3	I/O	Data Input/Output
14	VSS	-	Ground
15	I/O4	I/O	Data Input/Output
16	I/O5	I/O	Data Input/Output
17	I/O6	I/O	Data Input/Output
18	I/07	I/O	Data Input/Output
19	I/O8	I/O	Data Input/Output
20	CS	I	Chip select Input
21	A10	I	Address input
22	OE	0	Out put enable
23	A11	I	Address input
24	A9	I	Address input
25	A8	I	Address input
26	A13	I	Address input
27	WE	I	Write Enable input
28	VDD	_	Power Supply

## 3. Truth table

CS	OE	WE
Н	Х	Х
L	н	Н
L	Н	н
L	L	н
L	Х	L

# < MEMO >



